INSTRUCTION MANUAL

MODEL CTLR10/S2-S6 and CTLR10P/S2-S6

SOLENOID CONTROLLERS (EXCITERS)

(FOR SERIAL NO. 201 AND UP)

SCANIVALVE CORP.
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INSTRUCTION MANUAL

FOR

CTLR10/S2-S6 and CTLR10P/S2-S6

INDEX

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GLOSSARY

DEFINITIONS, ABBREVIATIONS AND ACRONYMS

bit--Abbreviation for binary digit. A unit of information equal to one binary decision.

channel encoder--A subassembly which generates position information.

CMOS--Complementary metal-oxide semiconductor (e.g., CMOS IC's).

constant current source--A source of fixed current which is used in power supplies and to supply power to LED's.

CTLR--Solenoid controller.

DSS--Double Scanivalve System.

dummy p-ducer--A solid metal device, with the same physical shape as an actual p-ducer, which has a hole thru its center that is terminated with a .063 O.D. tubulation. It fits into the Scanivalve p-ducer cavity in place of the actual p-ducer. This dummy p-ducer allows the use of an external transducer with the Scanivalve.

E-P transducer--Electrical signal to pressure transducer (usually current to pressure).

FF--Flip-flop.

F.S.--Full scale.

home cycle--The logic sequence that the XSS goes thru to cause the XSS to advance to the Scanivalve home port. Consists of a sequence of step cycles.

home mode--The state in which the XSS is in when a home cycle is being executed.

IC--Integrated circuit (e.g., analog or digital IC's).

interface--The junction between systems or subsystems where information is transferred from one system to another system.

I-P transducer--Current to pressure transducer.

LED-Light emitting diode. A solid state diode usually of gallium arsenide or gallium arsenide phosphide which emits light in the visible and/or infrared spectrum(s) when forward biased.

MOS--Metal oxide semiconductor (e.g., MOS transistors, MOS IC's).

MSS--Multiple Scanivalve System.

OCI--Optically coupled isolator. Normally consists of an LED and a PT encapsulated in an opaque package. The package has an internal light passage between the LED and PT.

PCB--Printed circuit board.

p-ducer--Pressure to voltage transducer.

phasing--The relationship of the stepping motor, Scanivalve port openings and channel encoder to each other and to the electrical home position (Port 00).

position encoder--That part of the channel encoder which detects and processes the position information.

PT--Phototransistor. A transistor, with a transparent body or window, which is sensitive to light. It accepts light as an input signal and furnishes a voltage output. The base lead is often not available to the user. When the base lead is brought out, it may be used to adjust the sensitivity of the phototransistor using a voltage input.

quiescent--Steady state, the condition of the XSS and its circuits, with power applied and the XSS at rest.

RTL--Resistor transistor logic (IC's).

RTR--Ready-to-read. An output bit which indicates when the analog output is ready to sampled.

RTR Delay--An adjustable delay which has been provided to allow enough time for the analog output signal to stabilize. The term is commonly used to include the entire ready-to-read signal (i.e., motor running time plus the delay period).

signal conditioner--A power supply and/or amplifier used with the p-ducer. A power supply supplies the excitation for the p-ducer and the nominal millivolt output of the p-ducer is available. A power supply and amplifier (as an integral unit) supplies excitation for the p-ducer and conditions the millivolt output of the p-ducer to make a higher voltage output or a proportional current output available. Signal conditioners usually have integral zero balance and span adjust controls.

step cycle--The logic sequence that the XSS goes thru to cause the XSS to advance its position one Scanivalve port. Consists of a sequence of four pulses to the motor.

step mode--The state in which the XSS is in when a step cycle is being executed.

SSD--Single Scanivalve Distribuvalve.

SSS--Single Scanivalve System.

TTL--Transistor-transistor logic (IC's).

XSS--The Scanivalve Pneumatic Scanning System to which the manual applies.(e.g. SSS, DSS, SSD, etc.)

1.0 INTRODUCTION

The CTLR10/S2-S6 plugs into ac power and provides 24 volts (rms) of unfiltered, full-wave rectified dc power and a Power Gate suitable for stepping LEDEX solenoid drives. These LEDEX solenoid drives have been manufactured by ScanCo, since 1956, to turn (rotate) either fluid switch wafers or Scanivalves.

The CTLR10P/S2-S6 is a CTLR10/S2-S6 with a built-in pulser (intervalometer) added.

Both of the above are economical solenoid drive CTLRs which are capable of energizing LEDEX size S2 thru S6 solenoids. The CTLRs operate open loop and do not require the solenoid to be equipped with an auto-interrupter switch. This has the advantage of eliminating the arcing (explosion hazard) which normally accompanies the use of auto-interrupters with other CTLRs.

See M9.10 and M9.20 in the appendix for examples of other ScanCo CTLRs.

1.1 INSTALLATION NOTES

1. See section 3 for general installation instructions.
2. For Solenoid Drives with Fluid Switch Wafers, use drawing number 85041.
3. For Solenoid Drives with 24 port Scanivalves, use drawing number 85041 modified by drawing number 8840.
4. For Solenoid Drives with 48 port Scanivalves, use drawing number 85041 modified by drawing number 8792.

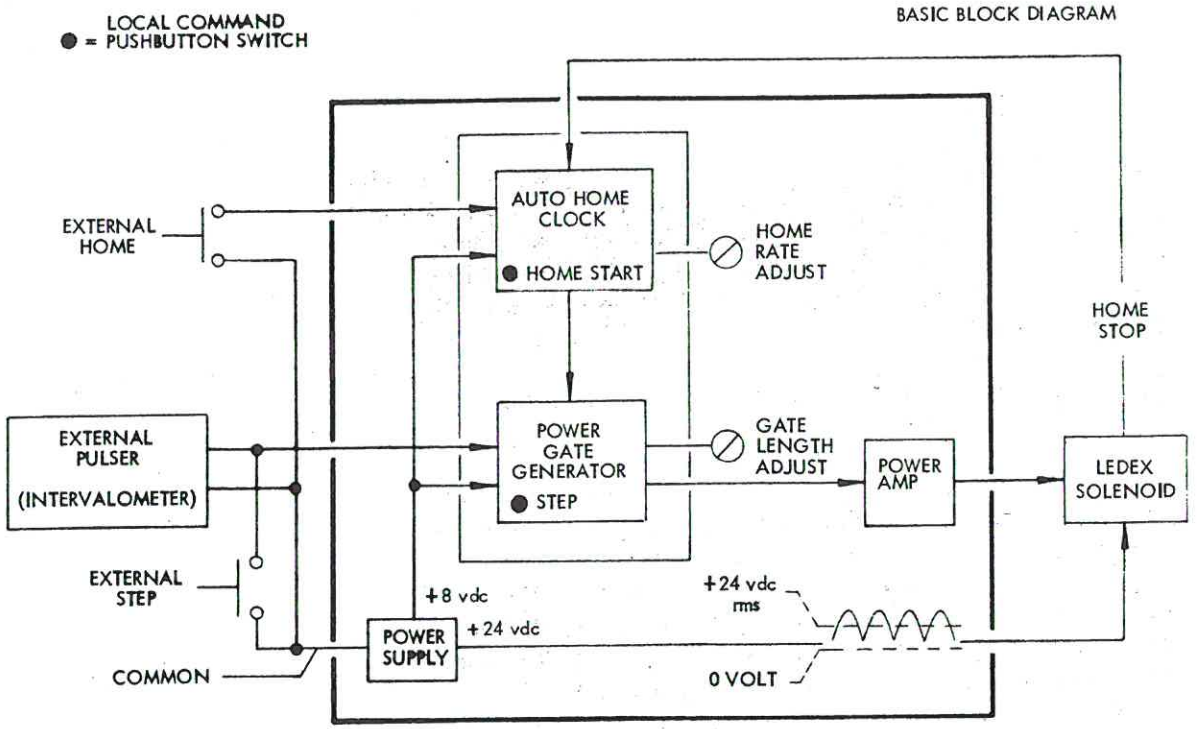


FIGURE 2.01 (CTLR10)

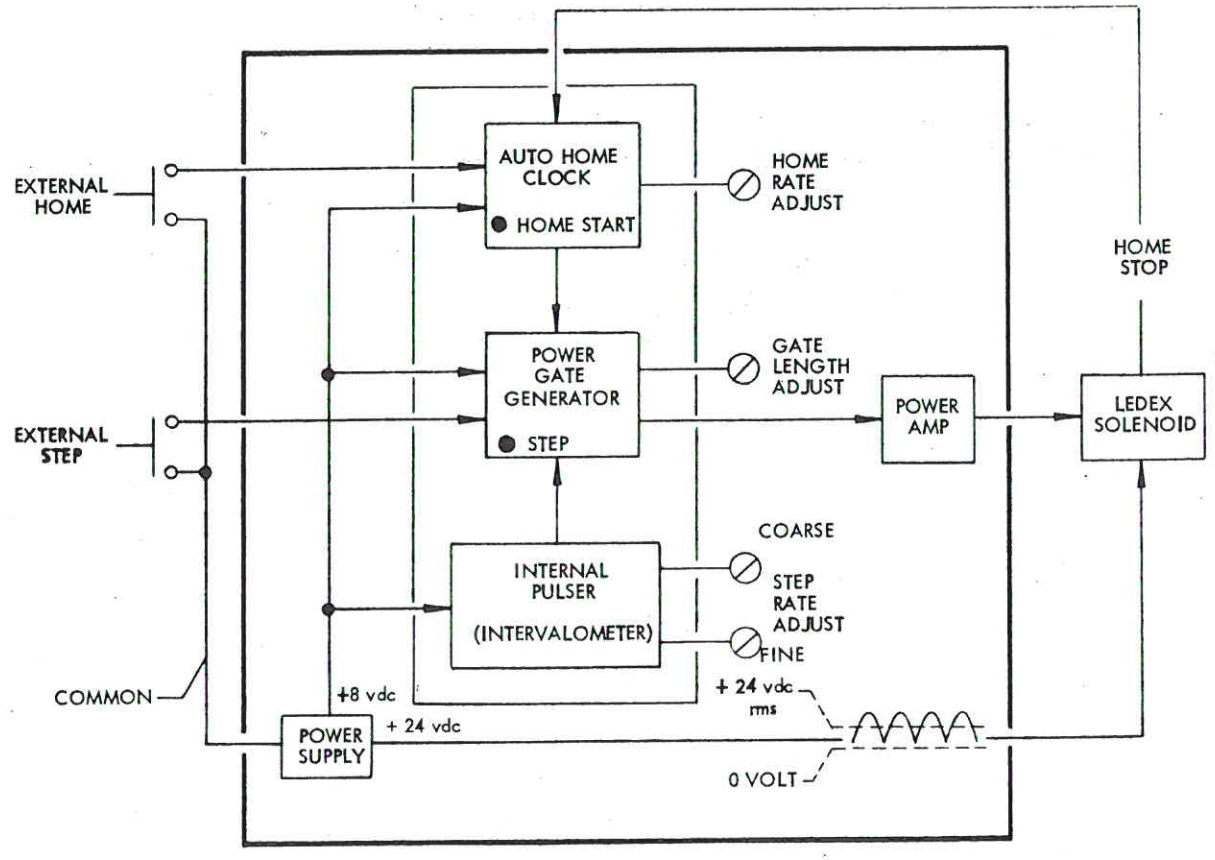


FIGURE 2.02 (CTLR10P)

FIG. 2.01 (CTLR10)/2.02 (CTLR10P)
75-12-3 CTLR10(P)/S2-S6

2.0 GENERAL DESCRIPTION

See Figure 2.01 & 2.02 for the basic block diagrams of the CTLRs.

2.1 INPUT COMMANDS

The CTLRs accept two types of input commands:

1. A Step Command, which advances the rotary solenoid drive one step, is given by the user thru the I/O terminal strip, TB101 (terminals 5 & 8), or by depressing the manual step command switch on the front panel.
2. A Home Command, which advances the rotary solenoid drive to the Home position, is given by the user thru the I/O terminal strip, TB101 (terminals 5 & 9), or by depressing the manual Home Command switch, on the front panel.

Both commands are switch or NPN transistor closures to signal common (TB101-5).

2.2 CONTROLS AND ADJUSTMENTS FOR CTLR10/S2-S6

There are three switches and two adjustments:

1. An ac power on/off switch, pilot light and fuse.
2. A local Step Command pushbutton switch.
3. A local Home Command pushbutton switch.
4. A Gate Length Adjust which allows the Power Gate to be adjusted from approximately 10 ms to 100 ms.
5. A Home Rate Adjust which allows the homing rate to be adjusted from approximately 6 steps/second to 20 steps/second.

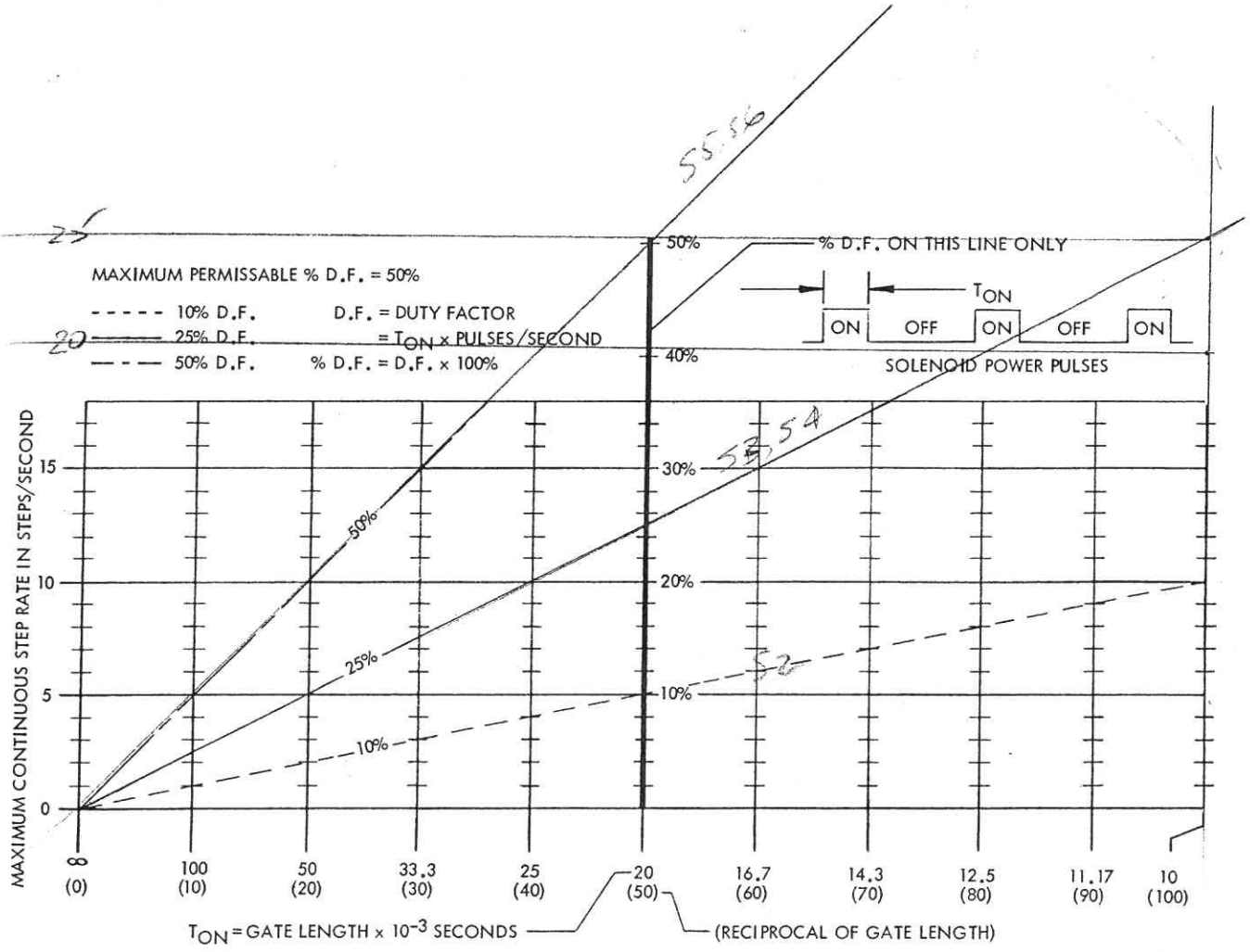
2.3 CONTROLS AND ADJUSTMENTS FOR CTLR10P/S2-S6

There are two switches and two adjustments in addition to those in the CTLR10/S2-S6:

1. A Pulser on/off switch.
2. A Step Rate Range selector, two position (fast/slow) switch, which allows a range of c.4 decades (10,000:1) to be covered.
3. The two Step Rate Adjust potentiometers (Coarse and Fine Adjust) allow the pulse rate of the Internal Pulser (intervalometer) to be adjusted over a span of c.2 decades or 100:1 (e.g. if the slowest rate is 1 step/8 seconds, the fastest rate will be c.12 steps/second).

2.4 ADJUSTMENTS

The maximum rate at which the rotary solenoid drive can be stepped or homed is limited by the setting of the Power Gate Length adjustment and the resultant duty cycle (heating) of the solenoid. The minimum usable gate length is determined by the size of the solenoid used and the load that is driven by the solenoid. The larger the solenoid and/or the larger the load, the longer the gate length must be for the CTLR to operate the solenoid reliably. The time between Power Gates must be as long or longer than the time the Power Gate is on. This is necessary to allow the solenoid to return to its rest (uncocked) position between Power Gates. See graph, Figure 2.41, for maximum step rates using different gate length and duty cycle variations.



GRAPH OF MAXIMUM CONTINUOUS STEP RATE VERSUS GATE LENGTH AND % DUTY FACTOR (% D.F.)

FIGURE 2.41

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAUTION: INSUFFICIENT WIRE SIZE USED BETWEEN CONTROLLER AND SOLENOID WILL REDUCE TORQUE.
2. THE FOLLOWING FORMULA OR TABLE 1 SHOULD BE USED TO PREVENT TORQUE LOSSES.

SCANIVALVE® CORP.

INSTRUCTIONS FOR WIRE SELECTION
CTLR2(P)/S2-S6 AND CTLR10P/S2-S6

DWN BY	DATE	SIGN BY		SHT
RCF	MAY 88	KP	85057	1 of 1

$$D = \frac{10\%\ Rs\ C}{2}$$

D = DISTANCE BETWEEN SOLENOID AND CONTROLLER (ft.)

Rs = SOLENOID RESISTANCE (Ω)

C = WIRE CONDUCTANCE (ft/Ω)

SOLENOID SIZE →		DISTANCE BETWEEN CONTROLLER AND SOLENOID FOR 10% DROP IN TORQUE				
WIRE GAGE	FT/Ω	S2 11.03Ω	S3 12.21Ω	S4 8.76Ω	S5 7.72Ω	S6 5.24Ω
30	9.7	5 ft.	6 ft.	4 ft.	4 ft.	2 ft.
26	24.5	13	15	11	10	6
22	62	34	38	27	24	16
20	98.5	54	60	43	38	25
18	156.5	86	95	68	60	41
16	249	137	152	108	96	65
14	397	218	242	173	152	103
12	629	384	374	272	242	164
10	1000	550	610	435	385	260
8	1592	876	971	692	613	414

TABLE 1

3.0 CHECKOUT AND OPERATION

3.1 CHECKOUT (Drawing No. 85041)

AC POWER: 115 or 230 vac, 50-60 Hz.

1. 115 vac: The CTLR is supplied with P101 molded to a standard (U.S.A.) 3-wire power cable.

   CAUTION: A CTLR supplied for 115 vac operation MUST NEVER BE OPERATED on 230 vac.

2. 230 vac: The CTLR is supplied with P101 molded to a 3-wire power cable approximately 12 inches long. The customer can splice on to the end of this cable or replace it with his own cable.

   Green wire -- Ground
   White wire -- Neutral
   Black wire -- Hot side of line.

3. After connecting the CTLR (to the CORRECT AC POWER) turn on the power switch. The pilot light should light and the CTLR is now ready to operate.

3.2 OPERATION

3.2.1 INPUT COMMANDS (Local)

1. Local Step Command: Depressing the local step command push button switch should cause the solenoid to advance one step.

2. Local Home Command: Depressing the local home command push button switch should cause the solenoid to advance to the Home position. Going from position 01 to Home takes approximately 2 to 10 seconds.

3.2.2 INPUT COMMANDS (Remote)

1. Remote Step Command: Using a wire to momentarily short between terminals 5 & 8 of TB101 should cause the solenoid to advance one step.

2. Remote Home Command: Using a wire to momentarily short between terminals 5 & 9 of TB101 should cause the solenoid to advance to the Home position, if the Home Stop contact is connected to terminals 5 & 7 of TB101.

FIG. 3.0 75-12-8
CTLR10P/S2-S6

FUNCTIONAL BLOCK DIAGRAM (CTLR10/S2-S6 & CTLR10P/S2-S6)

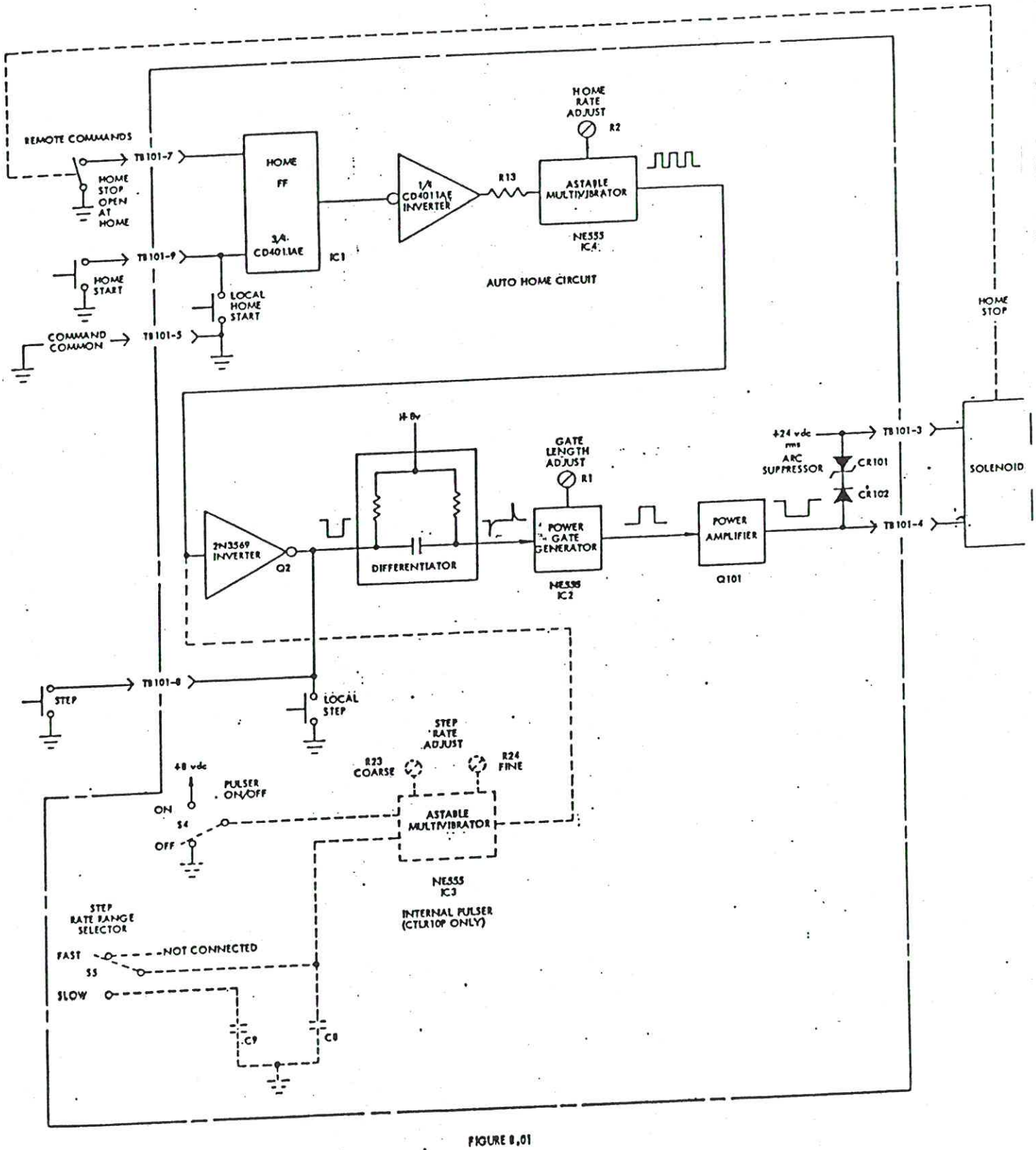


FIGURE 8.01

8.0 CONTROLLER CIRCUITS (See Figure 8.01)

The Controller circuits are divided into three major sub-assemblies:

1. Control Board (8.1)
2. Power Amplifier and Arc Suppressor (8.2)
3. Power Supply (section 9)

8.1 CONTROL BOARD

The Control board consists of four major subsections:

1. Input Filters (8.1.1)
2. Differentiator and Power Gate Generator (8.1.2)
3. Home FF & Clock (8.1.3)
4. Internal Pulser (CTLR10P only) (8.1.4)

8.1.1 INPUT FILTERS

Input filters are used on the Home and Home Stop command lines to prevent erratic operation during the Home cycle. C1, R3 & R5 are the Home input filter and C2, R4 & R6 are the Home Stop input filter.

8.1.2 DIFFERENTIATOR AND POWER GATE GENERATOR

The Step Command is accepted as a negative going pulse at the collector of inverter Q2, and differentiated by differentiator C5, R16 & R17. The negative pulse from the differentiator, which corresponds to the leading edge of the input pulse, triggers Power Gate Generator IC2.

IC2 is a monolithic timing circuit which can be used as either an astable or monostable multivibrator. In this application IC2 is used as a monostable. R1 is used to adjust the gate length of the Power Gate Generator. C6, R1 & R18 determine the gate length. C7 is the noise filter for the internal threshold reference. R19 limits the current from the output of IC2.

When the output of IC2 is high the Power Amplifier is turned on and energizes the solenoid. Each time the solenoid is energized it advances one step.

See "Astable and Monostable Multivibrators Using an IC (Monolithic) Timing Circuit" in the appendix.

8.1.3 HOME FF AND CLOCK

The Home Command is accepted as a negative going pulse at the set input of the Home FF. The Home FF consists of two cross coupled NAND gates, IC1-1 and IC1-4, with the Q output inverted by NAND gate IC1-2. When the output of IC1-2 is high it enables the clock.

See "Set-Reset FF" in the appendix.

The clock is a monolithic timing circuit used as an astable multivibrator. R2 is used to adjust the time between clock pulses. The output of the clock is inverted and fed thru the differentiator to the Power Gate Generator IC2. The operation of the rest of the circuit is identical to a Step Command (described in 8.1.2).

Since a Power Gate is generated for each clock pulse, a Home cycle consists of as many steps as are necessary to advance to the Home port position. The Home cycle is terminated when the Home contact (which is part of the electrical Home Wafer switch that is mounted on the LEDEX shaft) opens. No Home command will be accepted while this contact is open. IC1-3 inverts the Home STOP signal to reset the Home FF at Home.

8.1.4 INTERNAL PULSER (INTERVALOMETER) (CTLR10P only)

The Internal Pulser consists of a Step Rate Range selector switch, two Step Rate Adjust adjustments (coarse and fine), an astable multivibrator and an on/off switch.

The Step Rate Range selector switch is a two position toggle switch. The "up" position gives the fastest step rate and uses C8 as the timing capacitor. The "down" position gives the slowest step rate and places C9 in parallel with C8.

Two Step Rate Adjust potentiometers are used to allow easier adjustment and reduce the end effects of high resistance (1 meg) potentiometers. R23 (coarse adjustment) and R24 (fine adjustment) allow c.2 decades (100:1) of adjustment within each range. The span covered by using both range switch and rate adjustments is c.10 steps/second to 1 step/30 minutes or more than four decades of adjustment for the standard CTLR10P.

IC3 is a monolithic timing circuit used as an astable multivibrator. R23 & R24 are used to adjust the period of the pulser (time between beginning of pulses). C8, C9 (when in the circuit), R20, R21, R23 and R24 determine the step rate. C11 is the noise filter for the internal threshold reference. R22 limits the current from the output of IC3. When the output of IC3 goes high, the output of inverter Q2 goes low and is differentiated and used to trigger IC2. The pulser is disabled when S4 is closed to ground.

8.2 POWER AMPLIFIER AND ARC SUPPRESSOR

The Power Amplifier is a monolithic darlington transistor. When its input is high it energizes the solenoid and causes the solenoid to advance one step.

The Arc Suppressor consists of two diodes (CR101 & CR102) connected back-to-back across the solenoid power output terminals (terminals 3 & 4) of TB101. CR101 limits the maximum voltage across the solenoid and Power Amplifier (when the solenoid field is collapsing) to approximately 56 volts; CR102 prevents current flow thru CR101 when the Power Amplifier is on.

9.0 POWER SUPPLY

The Power Supply consists of three major subsections:

1. Transformer and Rectifier (9.1)
2. Decoupling Filter (9.2)
3. Voltage Regulator (9.3)

9.1 TRANSFORMER AND RECTIFIER

The transformer (T101) has dual primary and secondary windings. The two primary windings are connected in parallel (for 115 vac input) or series (for 230 vac input). This connection is determined by the jumpers used on terminal strip TB102. The two secondary windings are connected in series to obtain a 24 vac, center-tapped output winding.

CR1 thru CR4 on the Power Supply board form a full-wave bridge rectifier. The output of the bridge is $\approx$ 24 vdc, rms. $\approx$ 12 vdc, rms, is obtained from the center tap connection of T101's secondaries. This furnishes power for the regulator, via the filter.

9.2 DECOUPLING FILTER

C1 and CR5 form a decoupling filter on the Power Supply board. CR5 prevents dc on the secondary windings of T101 and prevents current drawn thru the solenoid from discharging C1. C1 developes $\approx$ 17 volts for regulator IC1.

9.3 VOLTAGE REGULATOR

The Power Supply has an 8 volt regulator which supplies power to the Control Board.

See "Power Supplies and Regulators" in the appendix.

10.0 EXTERNAL POWER CAPACITOR

Depending on torque and scan rate requirements, the CTLR10P/S2-S6 in the "As Sold" configuration sometimes will not adequately drive an S5 or S6 solenoid. When driving W62 wafers or more than three of any other model wafer on an S5 or S6 drive, the customer should always use a CTLR2 or CTLR2P. However, in those cases where the customer already has a CTLR10P, it may be used to drive an S5 or S6 solenoid providing (1) the scan rate is less than or equal to 2 ports/sec, and (2) the solenoid is wired to the controller with an additional resistor and capacitor as shown in Fig. 10.01.

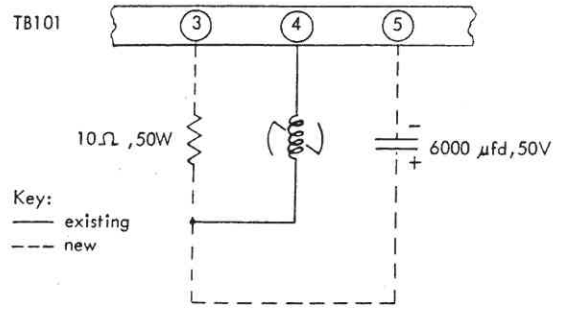


FIG. 10.01- EXTERNAL POWER CAPACITOR

INDEX TO APPENDIX

(SCHEMATICS AND MAPS)

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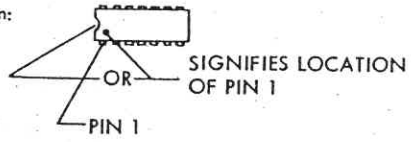
SCANIVALVE CORP.				
ELECTRICAL NOTES, STANDARDS (CUSTOMER)				
DWN BY JRA	DATE FEB 73	CKD BY	0014	SHT. 1 of 2

NOTE: UNLESS OTHERWISE SPECIFIED ON INDIVIDUAL DRAWINGS

1. Capacitance is expressed in uf, microfarads.
2. Resistance is expressed in Ω , ohms.
3. All wires are #22 AWG. PVC insulated (0987-22-XX)
4. All resistors are 1/4 watt, 10%.
5. —⌒— indicates a jumper. (x) indicates identified jumper point. (x represents identification)
6. Schematic diagrams are drawn with the inputs on the left and the outputs on the right.
7. All NPN transistors are 2N3569. All PNP transistors are 2N3638.
8. ◪ denotes "track" on optical encoding disc.
9. f = farad, s = second, and w = watts.
10. MEG = mega (10^6), K = kilo (10^3), m = milli (10^{-3}), u = micro (10^{-6}), n = nano (10^{-9}) and p = pico (10^{-12}).
11. All diodes are 1N600.
12. I.C. identification:



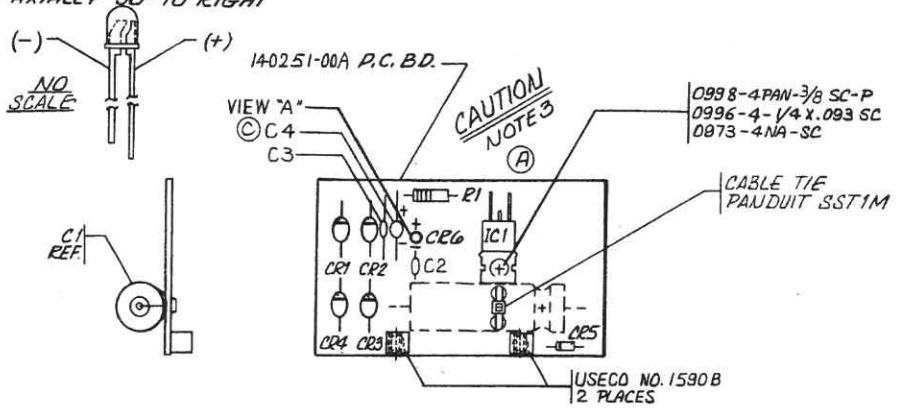
13. On non-plated thru boards:
    use jumpers indicated by ⊕ ; solder top at points indicated by ■.
14. On plated thru boards fill in holes with solder indicated by ⊗ .
15. Letters are located on the top or component side; numbers on the bottom or circuit side.
16. Broken lines - - - for optional components & circuitry on the board.
17. Long with one short for board outlines ——— – ——— (.020 thick)
18. Long with two shorts for groups of identified components ——— – – ——— (.010 thick)
19. Heavy solid line (.030 thick) for perimeter of major subassemblies.
20. ———→ + VDC indicates VDC circuitry.
21. —⏚— indicates ground circuitry (or common). Also —▽— where x indicates a common ground point when more than one ground point is used to reduce noise and/or ground loops (currents).
22. IN — [XX VOLTAGE REGULATOR] — OUT ⏚ Indicates a functional block consisting of a monolithic or hybrid regulator which has been adjusted for the indicated voltage. For further details see "Power Supplies and Regulators" in the Appendix.
23. ▒ Shaded area, when present, indicates modifications for kits.
24. →)— Indicates male & female connectors respectively.

NOTE : UNLESS OTHERWISE SPECIFIED

1. RUBBER STAMP SA NUMBER TO SOLDERED SIDE OF COMPLETED BOARD
2. SEE WIRING DIAG. NO. 85041 FOR SCHEM. DIAG.
3. IF IC1 = MC7805CP (B.U. IC-11C) REPLACE LED(CR6) WITH IN751A (B.U. CE-128) PER WIR. DIAG. 85041

SCANIVALVE® CORP.					
SA CTLR10P/S2-S6 POWER SUPPLY BD.					
DWN BY SL	DATE AUG 72	CKD BY	140251 SHT. 1 of 3		MAP
A	ERC A-495 JRA JAN 74		C	ECNA-453HSHMAY81	P/L SHT. 2
B	ERC A-654 HSH AUG 77				

Ⓐ CR6 VIEW A
SIDE VIEW ~ ROTATED AXIALLY 90° TO RIGHT

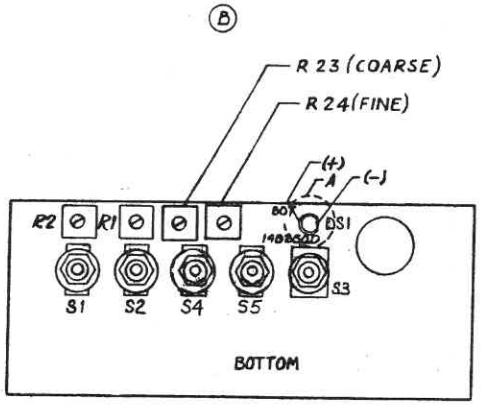


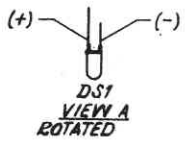
ⒸⒷⒶ -1A SA CTLR10P/S2-S6 POWER SUPPLY BD.

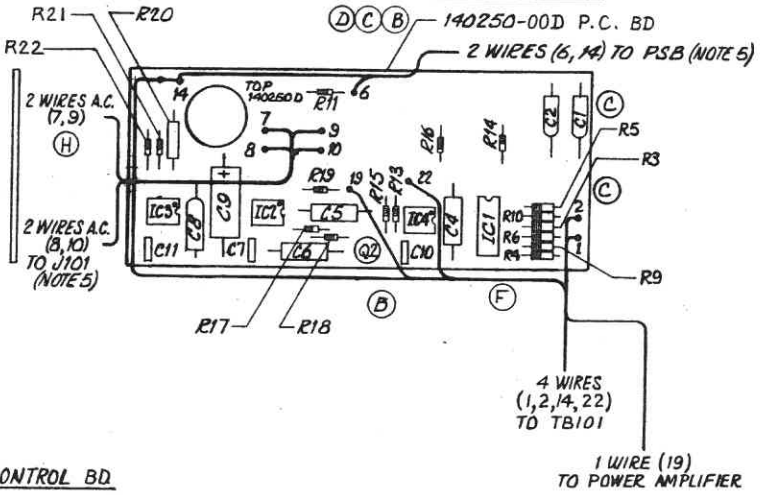
NOTE : UNLESS OTHERWISE SPECIFIED

1. ~~TWISTED LEAD LENGTHS & NUMBERS FOR LETTER BOTH ONLY (WIRE #AWG #TYP) (TYP NUMBER #)~~
2. * PSB INDICATES POWER SUPPLY BD. SA 140251-1
3. RUBBER STAMP SA NUMBER TO SOLDERED SIDE OF COMPLETED BOARD
4. SEE WIRING DIAG. #85041
5. WIRES TO BE TWISTED: B #10, 6 #14
6. ▲ INDICATES : NOTE LENGTH BEFORE TWISTING

FROM CONTROL BD	1	2	6 ▲	7 (H)	8 (H) ▲	9	10 ▲	14 ▲	14	19	22	FROM F101 -2 (H)
TO	TB101 -7	TB101 -9	PSB -6*	F101 -1	J101 -1	TB102 -4	J101 -2	TB101 -5	PSB -10*	POWER AMP. BASE	TB101 -8	TB102 -1
COLOR	BRN	RED	BLU	#20 BLK	#20 BLK	#20 WHT	#20 WHT	BLK	BLK	WHT	GRY	#20 BLK
LENGTH	9.0	8.5	16.0	6.0	27.0	14.5	17.0	18.5	16.5	13.5	11.0	17.5





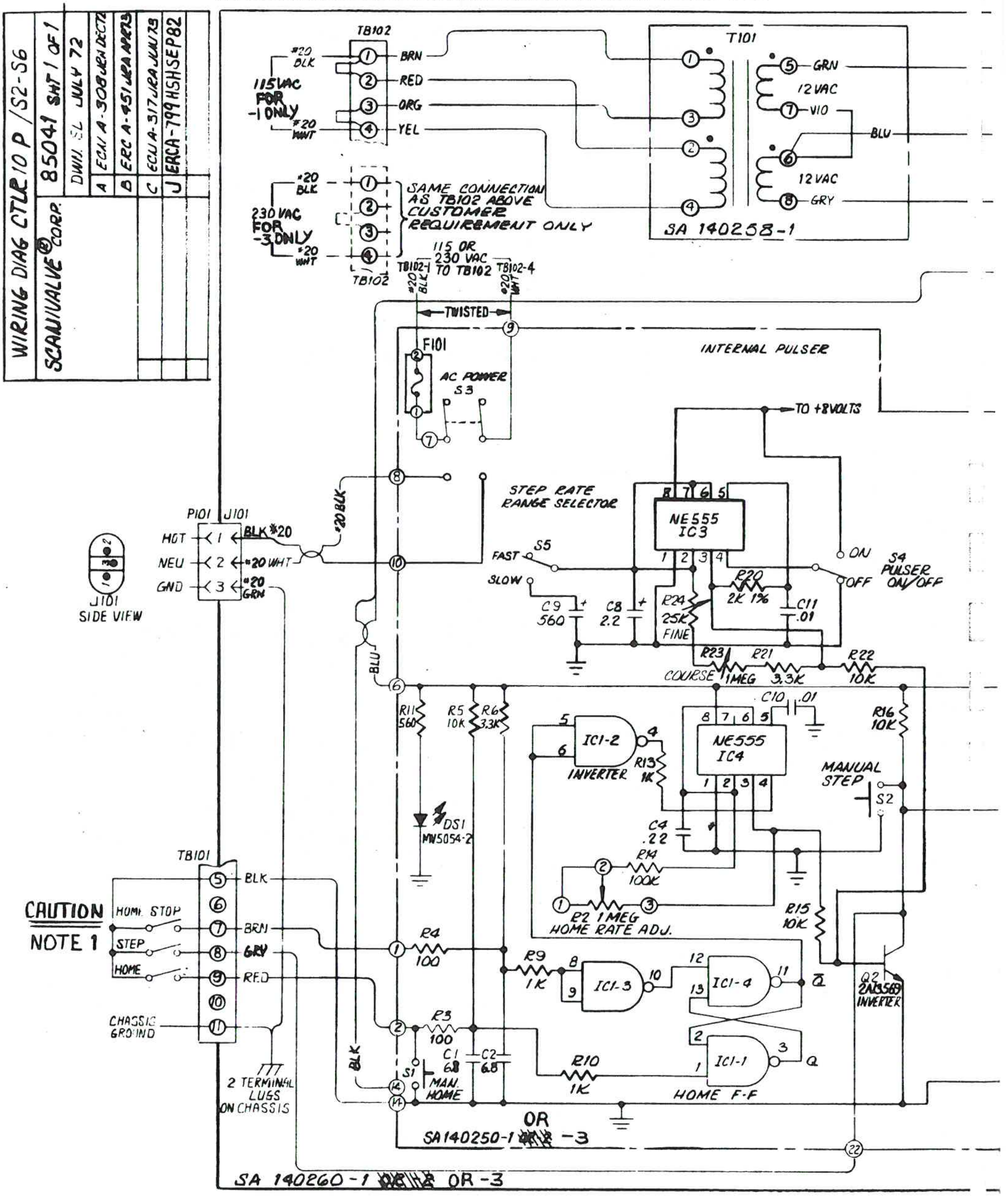


Ⓗ -1A SA CTLR 10 P/S2-S6 CONTROL BD

SCANIVALVE CORP.					
SA CTLR10P/S2-S6 CONTROL BD					
DWN BY SL	DATE AUG 72	CKD BY	140250 SHT. 1 of 4		MAP
H	ERCA-799 HSH SEP 82				P/L SHT 223

NOTE: UNLESS OTHERWISE SPECIFIED

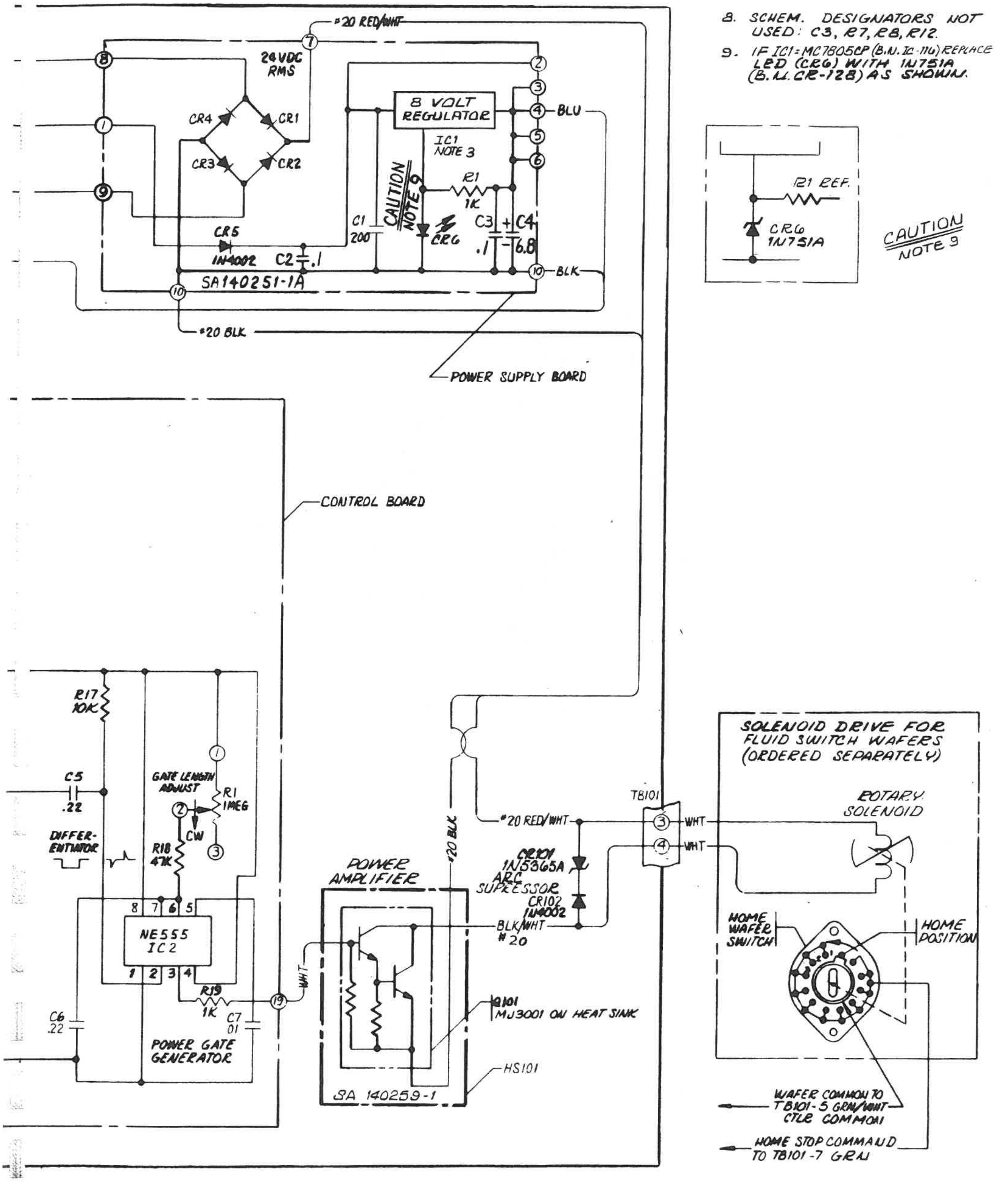
1. THIS HOME STOP CONTACT IS A DUPLICATE OF WAFER SWITCH SHOWN AT LOWER RIGHT. OPENS AT HOME.
2. VALUE FOR R21 IS TYPICAL. VALUE MAY CHANGE ±20% FOR COMPONENT TOLERANCES.
3. FOR ELECTRONIC NOTES USE DWG. NO. 0019, OTHER NOTES ARE THE EXCEPTIONS.



WIRING DIAG CTLR 10 P / S2-S6
85041 SHT 1 OF 1
DWN. SL JULY 72
SCANIVALVE® CORP.
A ECN A-308 JRA DEC72
B ERC A-451 JRA APR73
C ECN A-317 JRA JUL73
J ERCA-799 HSH SEP82
TB102
115VAC FOR -1 ONLY
230VAC FOR -3 ONLY
#20 BLK
#20 WHT
BRN
RED
ORG
YEL
SAME CONNECTION AS TB102 ABOVE CUSTOMER REQUIREMENT ONLY
115 OR 230 VAC TO TB102
TB102-1
TB102-4
TWISTED
T101
GRN
12 VAC
VIO
BLU
GRY
SA 140258-1
F101
AC POWER S3
INTERNAL PULSER
TO +8VOLTS
STEP RATE RANGE SELECTOR
NE555 IC3
FAST
SLOW
S5
ON
OFF
S4 PULSER ON/OFF
C9 560
C8 2.2
R24 25K FINE
R20 2K 1%
C11 .01
R23 COURSE 1MEG
R21 3.3K
R22 10K
P101
J101
HOT
NEU
GND
BLK #20
#20 WHT
#20 GRN
J101 SIDE VIEW
#20 BLK
R11 560
R5 10K
R6 3.3K
IC1-2 INVERTER
R13 1K
C10 .01
NE555 IC4
R16 10K
MANUAL STEP S2
DS1 MV5054-2
C4 .22
R14 100K
R2 1MEG HOME RATE ADJ.
R15 10K
TB101
CAUTION NOTE 1
HOME STOP
STEP
HOME
BLK
BRN
GRY
RED
CHASSIS GROUND
R4 100
R9 1K
IC1-3
IC1-4
Q̄
Q2 2N3569 INVERTER
R3 100
C1 6.8
C2 6.8
R10 1K
IC1-1
Q
HOME F-F
S1 MAN. HOME
2 TERMINAL LUGS ON CHASSIS
OR
SA140250-1 OR-2 -3
SA 140260-1 OR-2 OR -3

4. INITIAL CLEAR CIRCUIT FOR POWER TURN ON CONSISTS OF C3, R1, & R8
5. ~~SOLID LINES INDICATES CIRCUITRY FOR 140250-2 FOR 87LR10. PHANTOM LINES INDICATES CIRCUIT ADDED TO 140250-2 FOR 140251-1 (FOR 87LR10P)~~
6. CR1 THRU CR4 = 1N5625
7. ⊐⊏ INDICATES TWISTED LEADS

8. SCHEM. DESIGNATORS NOT USED: C3, R7, R8, R12.
9. IF IC1 = MC7805CP (B.N. IC-116) REPLACE LED (CR6) WITH 1N751A (B.N. CR-128) AS SHOWN.

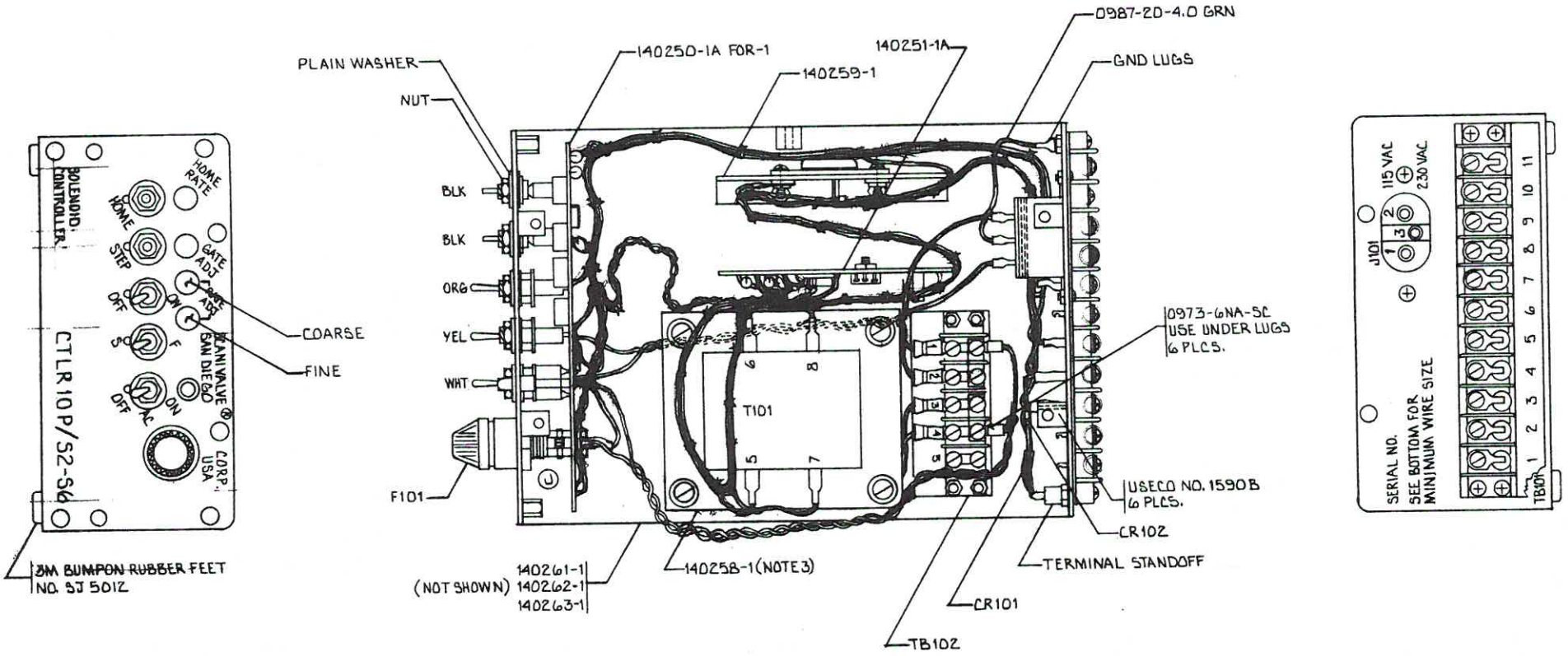


#20 RED/WHT
24VDC
RMS
8 VOLT REGULATOR
BLU
CR4
CR1
CR3
CR2
IC1
NOTE 3
CAUTION
NOTE 9
R1
1K
C1
200
CR6
C3
.1
C4
6.8
CR5
1N4002
C2 .1
BLK
SA140251-1A
#20 BLK
POWER SUPPLY BOARD
R1 REF.
CR6
1N751A
CAUTION
NOTE 9
CONTROL BOARD
R17
10K
C5
.22
GATE LENGTH ADJUST
R1
1MEG
CW
DIFFER-ENTIATOR
R18
47K
NE555
IC2
R19
1K
C6
.22
C7
.01
POWER GATE GENERATOR
WHT
POWER AMPLIFIER
#20 BLK
Q101
MJ3001 ON HEAT SINK
HS101
SA 140259-1
#20 RED/WHT
CR101
1N5365A
ARC SUPRESSOR
CR102
1N4002
BLK/WHT
#20
TB101
WHT
WHT
SOLENOID DRIVE FOR FLUID SWITCH WAFERS (ORDERED SEPARATELY)
ROTARY SOLENOID
HOME WAFER SWITCH
HOME POSITION
WAFER COMMON TO TB101-5 GRN/WHT- CTLR COMMON
HOME STOP COMMAND TO TB101-7 GRN

NOTES: UNLESS OTHERWISE SPECIFIED

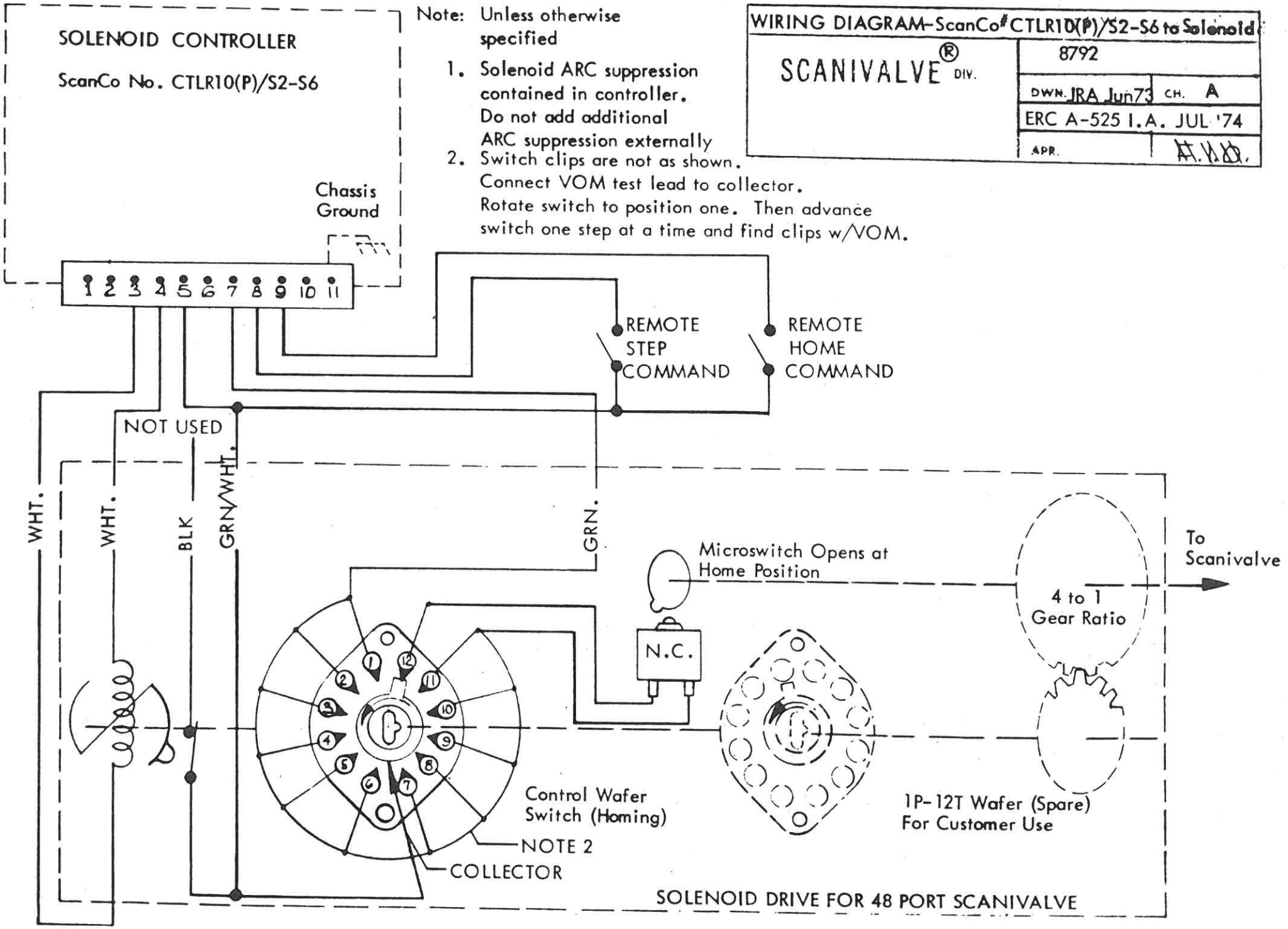
1. SEE WIRING DIAG. # 85041
2. 115 VAC OR 230 VAC PER CUSTOMER REQUIREMENT
3. USE LOCTITE ON TRANSFORMER SCREWS AT BOTTOM OF CHASSIS.

SCANIVALVE® CORP.				MAP
SA CTLR 10 P/S2-S6				P/L
RE-	DWN BY RCF	DATE SEPT 82	CKD BY	140260 SHT. 1 of 3
J	ERCA-795 RCF SEPT 82			SHT
				2&3



(J) -1 SA CTLR 10 P/S2-S6 (NOTE 3) (115 VAC)

(J) -2 SA CTLR 10 P/S2-S6 (230 VAC)


SOLENOID CONTROLLER
ScanCo No. CTLR10(P)/S2-S6
Note: Unless otherwise specified
1. Solenoid ARC suppression contained in controller. Do not add additional ARC suppression externally
2. Switch clips are not as shown. Connect VOM test lead to collector. Rotate switch to position one. Then advance switch one step at a time and find clips w/VOM.
WIRING DIAGRAM-ScanCo# CTLR10(P)/S2-S6 to Solenoid
SCANIVALVE® DIV.
8792
DWN. JRA Jun73 CH. A
ERC A-525 I.A. JUL '74
APR.
Chassis Ground
1 2 3 4 5 6 7 8 9 10 11
REMOTE STEP COMMAND
REMOTE HOME COMMAND
NOT USED
WHT.
WHT.
BLK
GRN/WHT.
GRN.
Microswitch Opens at Home Position
N.C.
To Scanivalve
4 to 1 Gear Ratio
Control Wafer Switch (Homing)
NOTE 2
COLLECTOR
1P-12T Wafer (Spare) For Customer Use
SOLENOID DRIVE FOR 48 PORT SCANIVALVE

NOTES UNLESS OTHERWISE SPECIFIED

SCANIVALVE® CORP.

WIRING DIAG. SCANCO NO. CTLR 10P/S2-S6
12 PORTS (S5 & S6 SOLENOID DRIVE)

DWN BY	DATE	CKD BY		
HE	NOV81		8849	SHT. 1 of 1

A	PER KP HSH JUN 82		

SOLENOID CONTROLLER
ScanCo No. CTLR 10P/S2-S6

Chassis Ground

1 2 3 4 5 6 7 8 9 10 11

Remote Step Command

Remote Home Command

NOT USED

WHT

WHT.

WHT/BLK

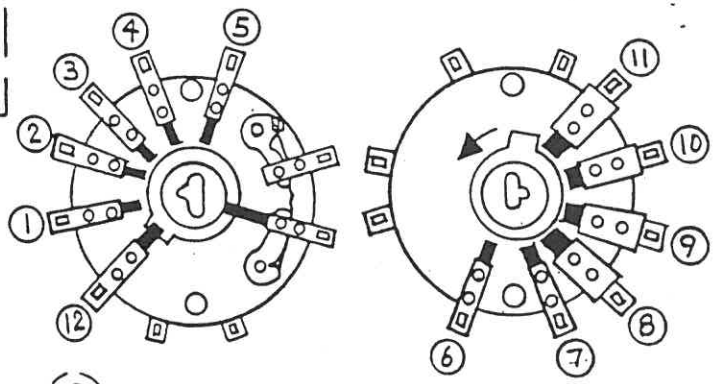
WHT/GRN

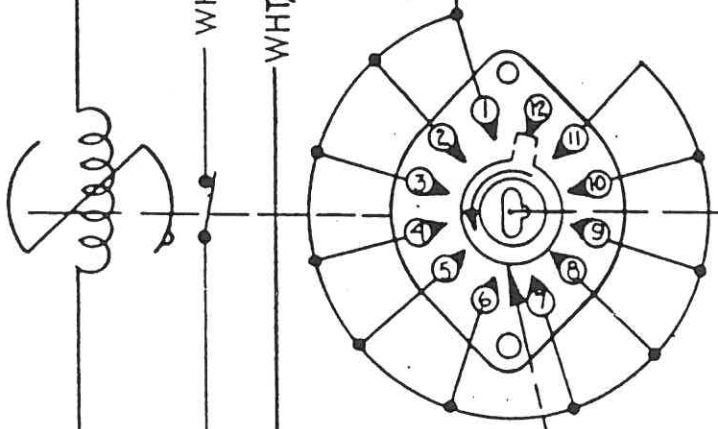
GRN.

HOME CONTROL WAFER (FOR S5 & S6 ONLY)

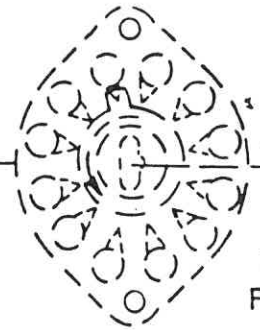
SOLENOID END VIEW

SHAFT END VIEW





Control Wafer Switch (Homing)



1P-12T Wafer (Spare) For Customer Use

To Scanivalve

SOLENOID DRIVE

CAUTION: SOLENOID ARC SUPPRESSION CONTAINED IN CONTROLLER.
DO NOT ADD ADDITIONAL ARC SUPPRESSION EXTERNALLY.

NOTES UNLESS OTHERWISE SPECIFIED

CAUTION: Solenoid arc suppression contained in controller. Do not add additonal arc supperssion externally.

	SCANIVALVE® CORP.			
	WIRING DIAG. SCAN CO NO. CTLR10P/S2-S6 FOR 24 PORTS (S5 & S6 SOLENOID DRIVE)			
DWN BY RCF	DATE OCT 81	CKD BY	8850	SHT 1 of 1

SOLENOID CONTROLLER
SCANCO NO. CRLR10P/S2-S6

CHASSIS GROUND

1 2 3 4 5 6 7 8 9 10 11

STEP

HOME

REMOTE COMMAND

NOT USED

WHT

WHT

WHT/BLK

WHT/GRN

GRN

HOME CONTROL WAFER

SOLENOID END VIEW

SHAFT END VIEW

TO SCANIVALVE

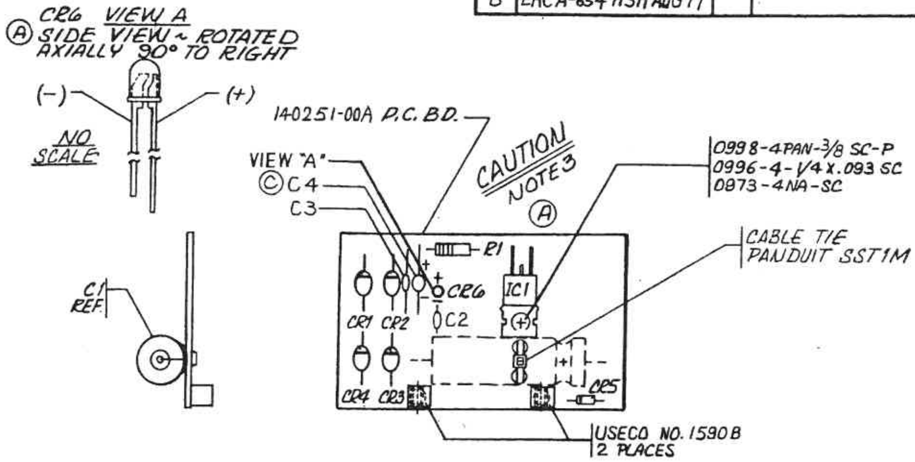
SOLENOID DRIVE

CONTROL WAFER SWITCH (24 PORTS)

1P-24T WAFER SWITCH FOR CUSTOME USE

NOTE: UNLESS OTHERWISE SPECIFIED
1. RUBBER STAMP SA NUMBER TO SOLDERED SIDE OF COMPLETED BOARD
2. SEE WIRING DIAG. NO. 85041 FOR SCHEM. DIAG.
(A) 3. IF IC1 = MC7805CP (B.M. IC-116) REPLACE LED (CR6) WITH 1N751A (B.M. CR-128) PER WIR. DIAG. 85041

SCANIVALVE® CORP.					
SA CTLR10P/S2-S6 POWER SUPPLY BD.					
DWN BY SL	DATE AUG'72	CKD BY	140251 SHT. 1 of 3		MAP
A	ERC A-495 JRA JAN74	C	ECNA-453HSHMAY81		P/L SHT. 2
B	ERCA-654 HSH AUG77				

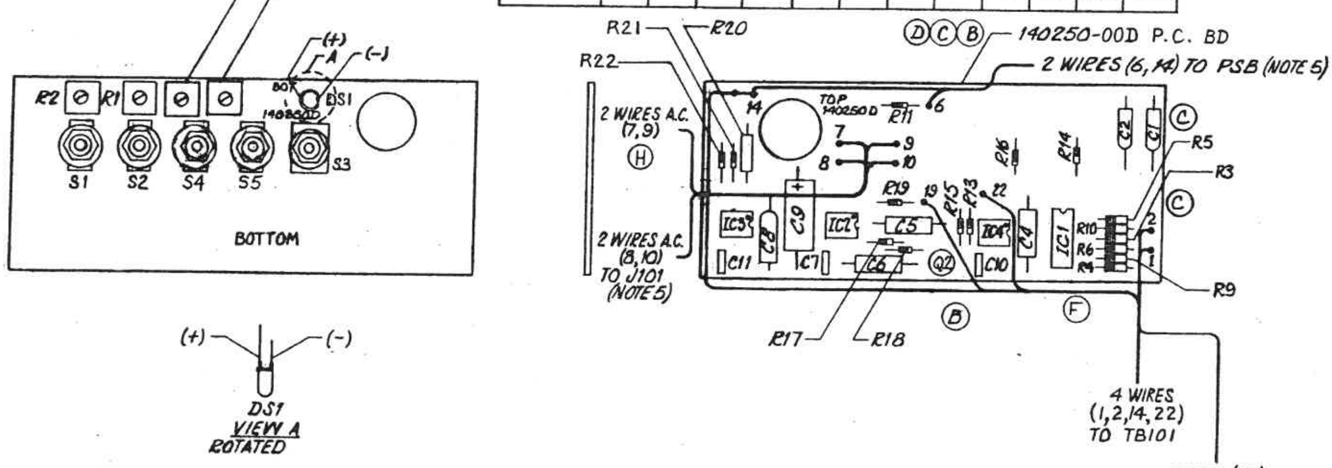


(C)(B)(A) -1A SA CTLR10P/S2-S6 POWER SUPPLY BD.

SCANIVALVE® CORP.				
SA CTLR10P/S2-S6 CONTROL BD				
DWN BY SL	DATE AUG'72	CKD BY	140250 SHT. 1 of 4	MAP
H	ERCA-799 HSH SEP82			P/L SHT 2&3

NOTE: UNLESS OTHERWISE SPECIFIED
~~1. [illegible]~~
2. * PSB INDICATES POWER SUPPLY BD. SA 140251-1
3. RUBBER STAMP SA NUMBER TO SOLDERED SIDE OF COMPLETED BOARD
4. SEE WIRING DIAG. #85041
5. WIRES TO BE TWISTED: 8 & 10, 6 & 14
6. ▲ INDICATES: NOTE LENGTH BEFORE TWISTING

FROM CONTROL BD	1	2	6 ▲	7 (H)	8 (H) ▲	9	10 ▲	14 ▲	14	19	22	FROM F101 -2 (H)
TO	TB101 -7	TB101 -9	PSB -6 *	F101 -1	J101 -1	TB102 -4	J101 -2	TB101 -5	PSB -10 *	POWER AMP. BASE	TB101 -8	TB102 -1
COLOR	BRN	RED	BLU	#20 BLK	#20 BLK	#20 WHT	#20 WHT	BLK	BLK	WHT	GRY	#20 BLK
LENGTH	9.0	8.5	16.0	6.0	27.0	14.5	17.0	18.5	16.5	13.5	11.0	17.5



(B)
R 23 (COARSE)
R 24 (FINE)
(+)
A
(−)
R2 R1
DS1
S1 S2 S4 S5 S3
BOTTOM
(+) (−)
DS1
VIEW A ROTATED
R21
R20
R22
(D)(C)(B) 140250-00D P.C. BD
2 WIRES (6, 14) TO PSB (NOTE 5)
2 WIRES A.C. (7, 9)
(H)
TOP 140250D
R11
R16
R14
C2
C1
(C)
R5
R3
R19
R15
R13
IC3
C8
C9
IC2
C5
IC4
C4
IC1
R10
R6
R4
R9
2 WIRES A.C. (8, 10) TO J101 (NOTE 5)
C11
C7
C6
Q2
C10
R17
R18
(B)
(F)
4 WIRES (1, 2, 14, 22) TO TB101
1 WIRE (19) TO POWER AMPLIFIER

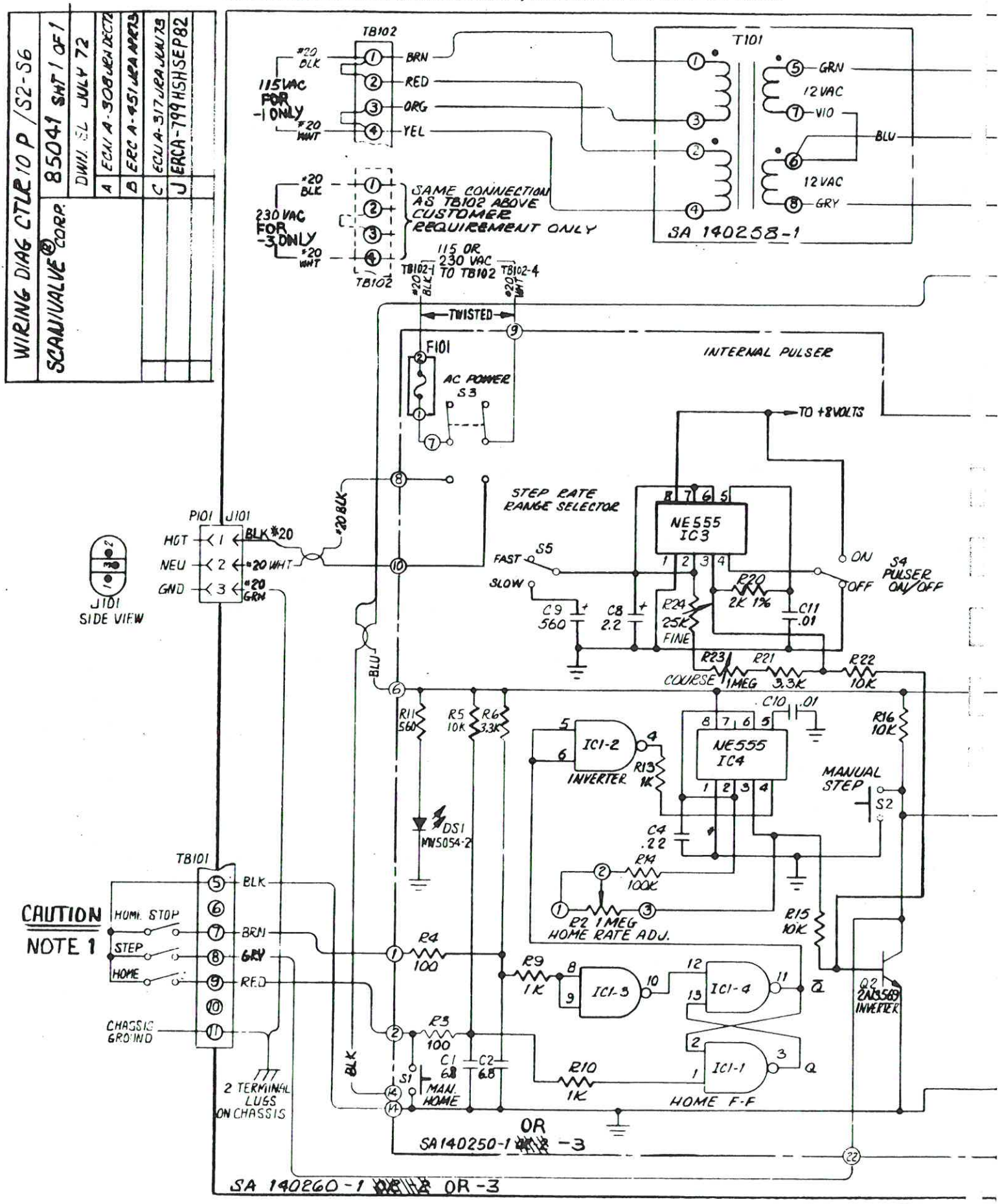
(H) -1A SA CTLR 10 P/S2-S6 CONTROL BD

NOTE: UNLESS OTHERWISE SPECIFIED

1. THIS HOME STOP CONTACT IS A DUPLICATE OF WAFER SWITCH SHOWN AT LOWER RIGHT. OPENS AT HOME.
2. VALUE FOR R21 IS TYPICAL. VALUE MAY CHANGE ± 20% FOR COMPONENT TOLERANCES.
3. FOR ELECTRONIC NOTES USE DWG. NO. 0014, OTHER NOTES ARE THE EXCEPTIONS.

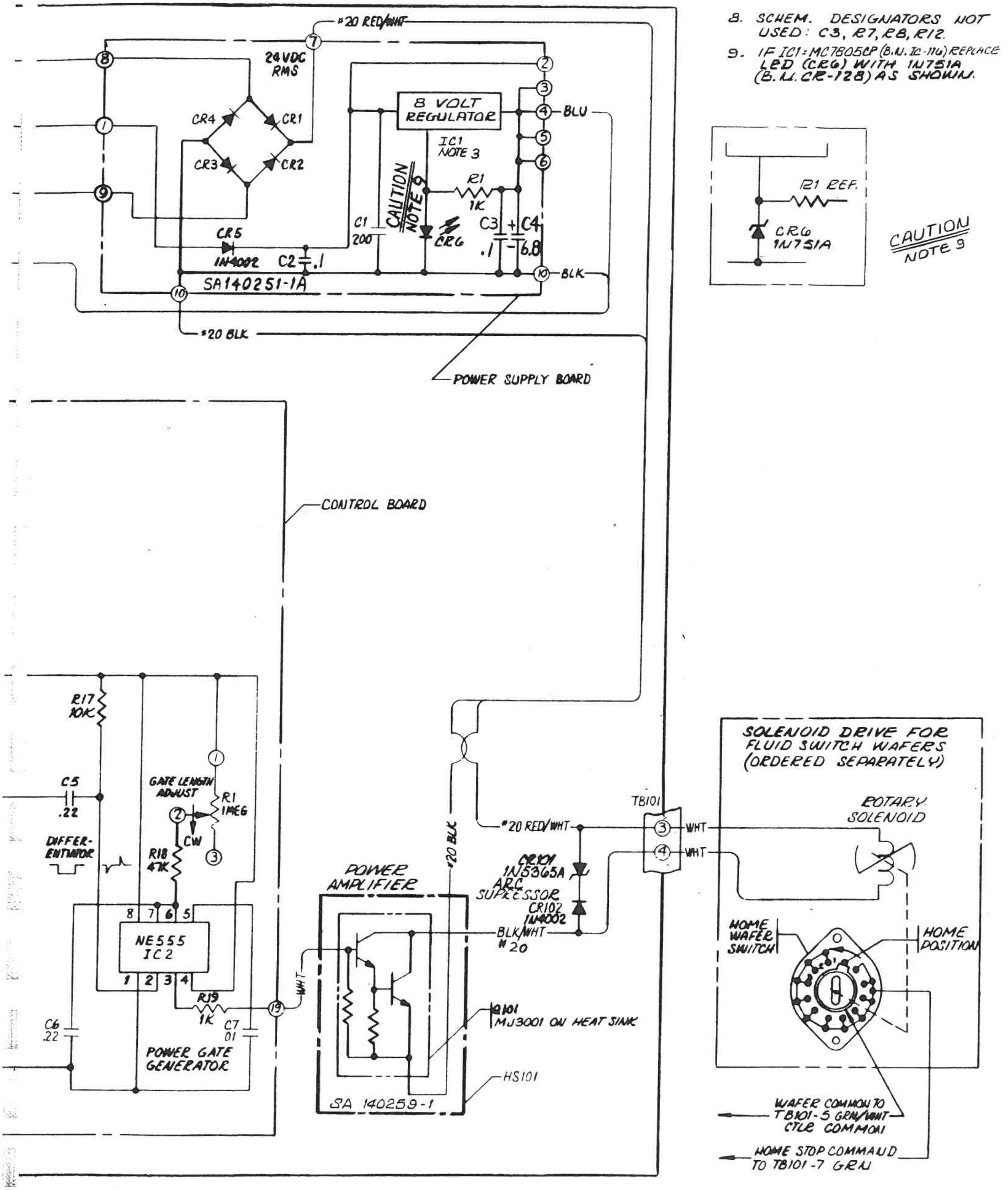
WIRING DIAG CTLR 10 P /S2-S6
SCANIVALVE® CORP.
85041 SHT 1 OF 1
DWN. SL JULY 72

A	ECN A-308 JUN 26/73
B	ERC A-451 JUN 27/73
C	ECN A-317 JUN 29/73
J	ERCA-799 H SHSEP 82



4. INITIAL CLEAR CIRCUIT FOR POWER TURN ON CONSISTS OF C3, R1, & R8
5 ~~SOLID LINES INDICATES CIRCUITRY FOR 140250-2 (FOR CTLR10). PHANTOM LINES INDICATES CIRCUIT ADDED TO 140250-2 FOR 140252 (FOR CTLR10R)~~
6. CR1 THRU CR4 = IN5625
7. ⊃⊂ INDICATES TWISTED LEADS

8. SCHEM. DESIGNATORS NOT USED: C3, R7, R8, R12.
9. IF IC1 = MC7805CP (B.N. IC-116) REPLACE LED (CR6) WITH IN751A (B.N. CR-128) AS SHOWN.

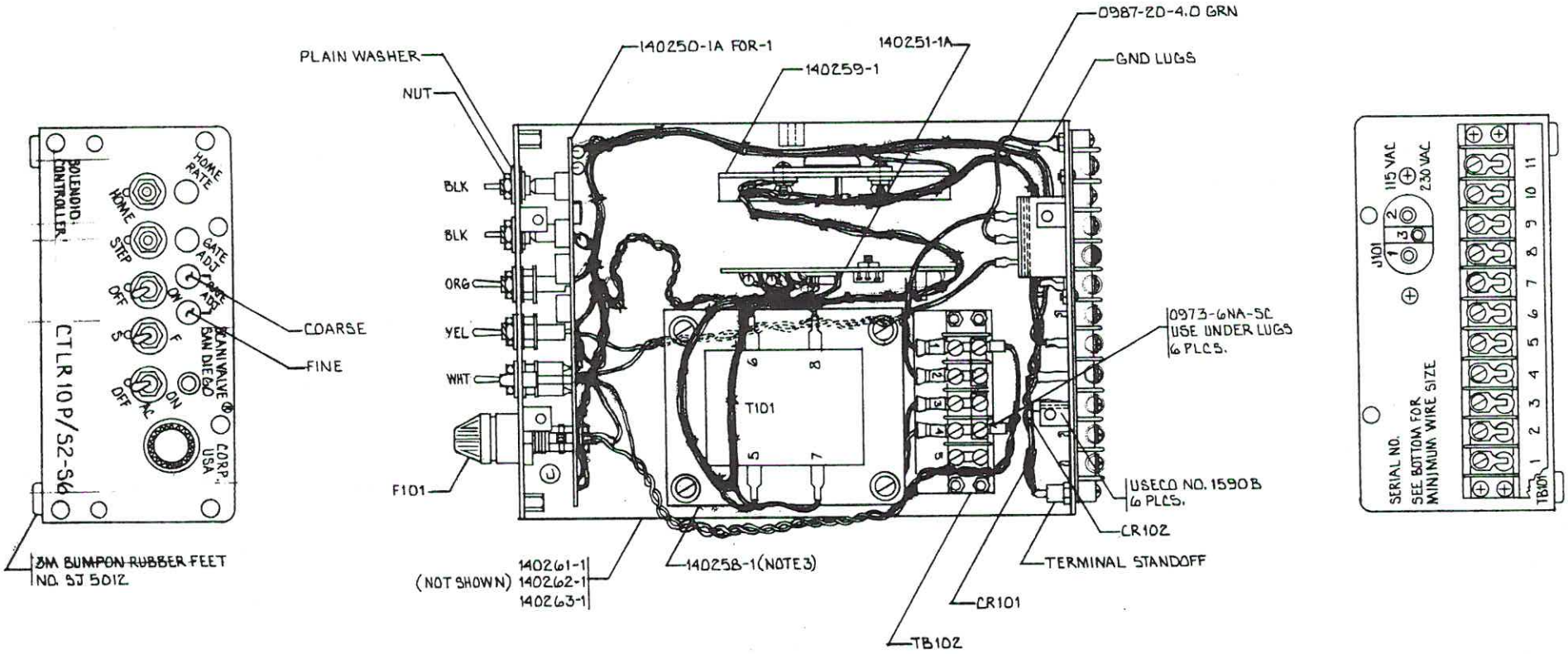


#20 RED/WHT
24VDC RMS
CR1
CR2
CR3
CR4
CR5
IN4002
C2 .1
C1 200
CAUTION NOTE 9
8 VOLT REGULATOR
IC1 NOTE 3
R1 1K
CR6
C3 .1
C4 6.8
BLU
BLK
SA140251-1A
#20 BLK
POWER SUPPLY BOARD
R21 REF.
CR6 IN751A
CAUTION NOTE 9
CONTROL BOARD
R17 10K
C5 .22
DIFFER-ENTIATOR
GATE LENGTH ADJUST
R1 IMEG
CW
R18 47K
NE555 IC2
R19 1K
C6 .22
C7 .01
POWER GATE GENERATOR
WHT
POWER AMPLIFIER
#20 BLK
SA 140259-1
Q101 MJ3001 ON HEAT SINK
HS101
#20 RED/WHT
CR101 IN5365A ARC SUPPRESSOR
CR102 IN4002
BLK/WHT #20
TB101
WHT
SOLENOID DRIVE FOR FLUID SWITCH WAFERS (ORDERED SEPARATELY)
ROTARY SOLENOID
HOME WAFER SWITCH
HOME POSITION
WAFER COMMON TO TB101-5 GRN/WHT CTLR COMMON
HOME STOP COMMAND TO TB101-7 GRN

NOTES: UNLESS OTHERWISE SPECIFIED

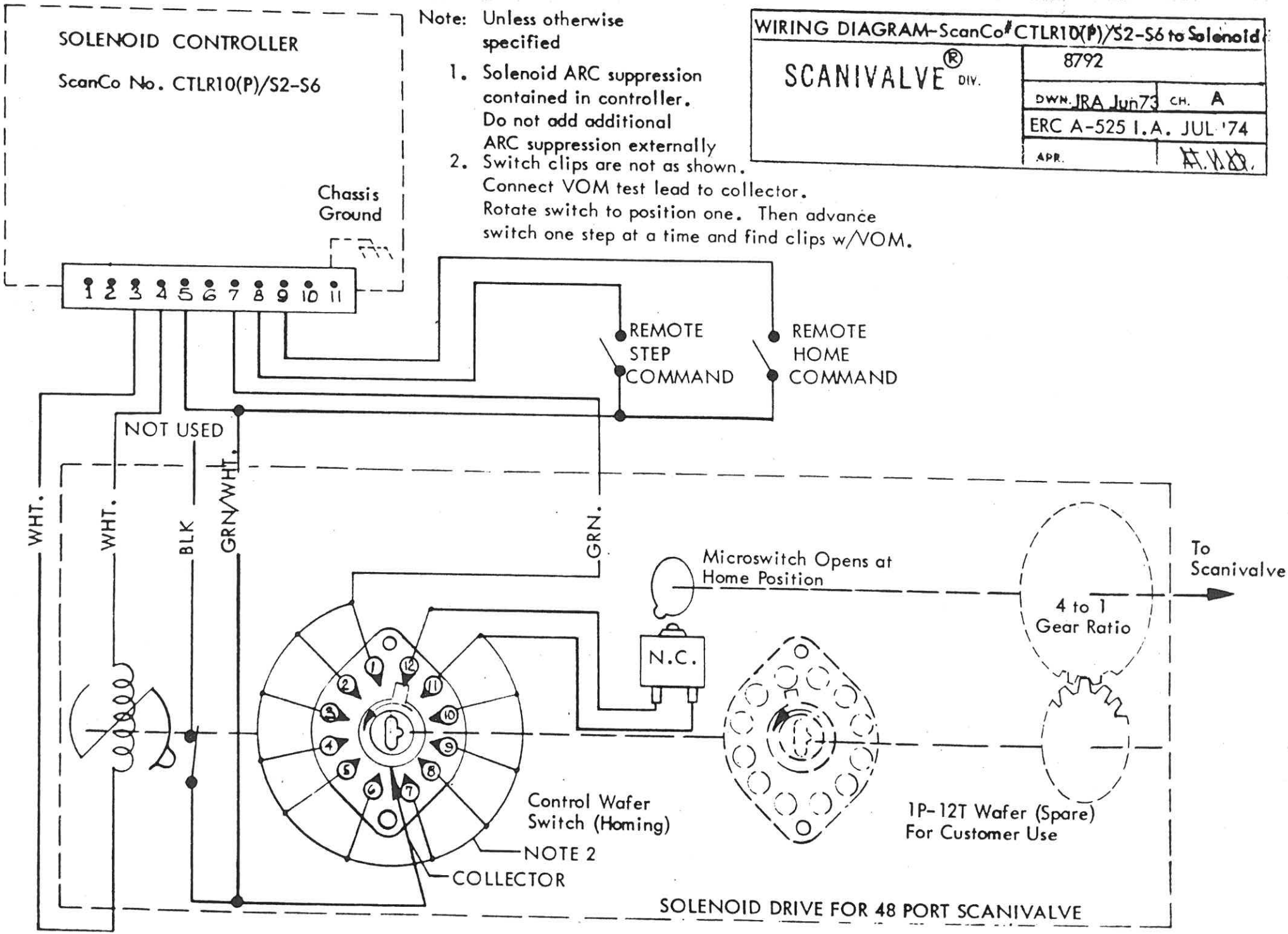
1. SEE WIRING DIAG. # 85041
2. 115 VAC OR 230 VAC PER CUSTOMER REQUIREMENT
3. USE LOCTITE ON TRANSFORMER SCREWS AT BOTTOM OF CHASSIS.

	SCANIVALVE® CORP.			MAP
	SA CTLR 10 P/S2-S6			
RE	DWN BY RCF	DATE SEPT 82	CKD BY	140260 SHT. 1 of 3 P/L
	J	ERCA-799 RCF SEPT 82		SHT
				2&3



(J) -1 SA CTLR 10 P/S2-S6 (NOTE 3) (115 VAC.)

(J) -2 SA CTLR 10 P/S2-S6 (230 VAC.)


SOLENOID CONTROLLER
ScanCo No. CTLR10(P)/S2-S6
Note: Unless otherwise specified
1. Solenoid ARC suppression contained in controller. Do not add additional ARC suppression externally
2. Switch clips are not as shown. Connect VOM test lead to collector. Rotate switch to position one. Then advance switch one step at a time and find clips w/VOM.
WIRING DIAGRAM-ScanCo# CTLR10(P)/S2-S6 to Solenoid
SCANIVALVE® DIV.
8792
DWN. JRA Jun73 CH. A
ERC A-525 I.A. JUL '74
APR.
Chassis Ground
1 2 3 4 5 6 7 8 9 10 11
REMOTE STEP COMMAND
REMOTE HOME COMMAND
NOT USED
WHT.
WHT.
BLK
GRN/WHT.
GRN.
Microswitch Opens at Home Position
N.C.
4 to 1 Gear Ratio
To Scanivalve
Control Wafer Switch (Homing)
NOTE 2
COLLECTOR
1P-12T Wafer (Spare) For Customer Use
SOLENOID DRIVE FOR 48 PORT SCANIVALVE

NOTES UNLESS OTHERWISE SPECIFIED

SCANIVALVE® CORP.

WIRING DIAG. SCANCO NO. CTLR 10P /S2-S6
12 PORTS (S5 & S6 SOLENOID DRIVE)

DWN BY	DATE	CKD BY		
HE	NOV81		8849	SHT. 1 of 1
A	PER KP HSH JUN 82			

SOLENOID CONTROLLER
ScanCo No. CTLR 10P/S2-S6

Chassis Ground

1 2 3 4 5 6 7 8 9 10 11

Remote Step Command

Remote Home Command

NOT USED

WHT

WHT.

WHT/BLK

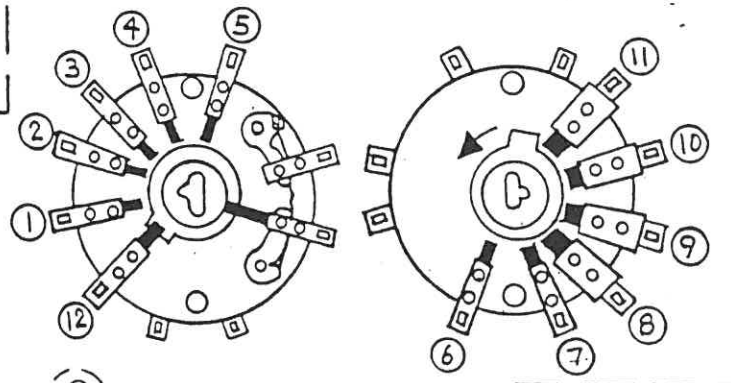
WHT/GRN

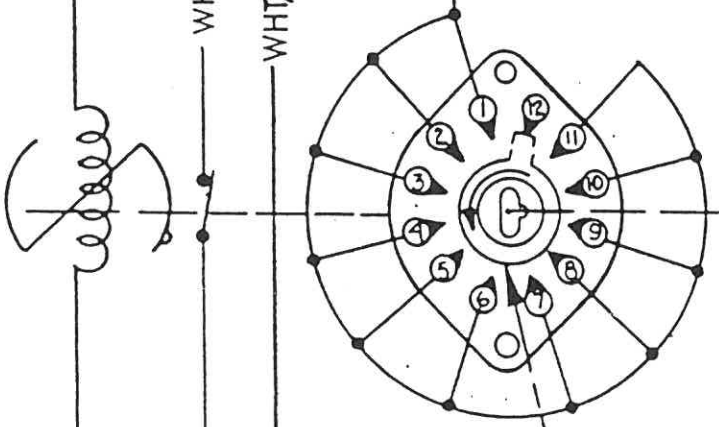
GRN.

HOME CONTROL WAFER (FOR S5 & S6 ONLY)

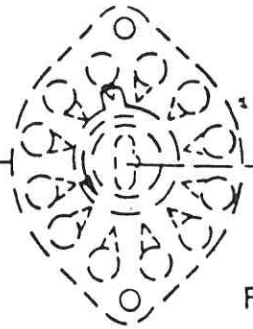
SOLENOID END VIEW

SHAFT END VIEW





Control Wafer Switch (Homing)



1P-12T Wafer (Spare) For Customer Use

To Scanivalve

SOLENOID DRIVE

CAUTION: SOLENOID ARC SUPPRESSION CONTAINED IN CONTROLLER.
DO NOT ADD ADDITIONAL ARC SUPPRESSION EXTERNALLY.

NOTES UNLESS OTHERWISE SPECIFIED

CAUTION: Solenoid arc suppression contained in controller. Do not add additonal arc supperssion externally.

SCANIVALVE® CORP.

WIRING DIAG. SCAN CO NO. CTLR10P/S2-S6 FOR 24 PORTS (S5 & S6 SOLENOID DRIVE)

DWN BY	DATE	CKD BY		
RCF	OCT 81		8850	SHT 1 of 1

SOLENOID CONTROLLER
SCANCO NO. CRLR10P/S2-S6

CHASSIS GROUND

1 2 3 4 5 6 7 8 9 10 11

STEP

HOME

REMOTE COMMAND

NOT USED

WHT

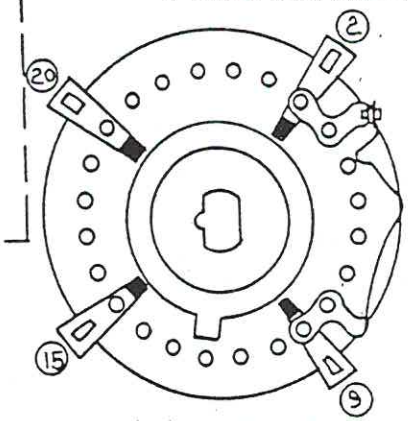
WHT

WHT/BLK

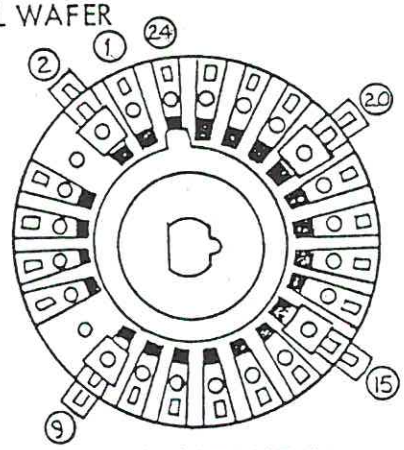
WHT/GRN

GRN

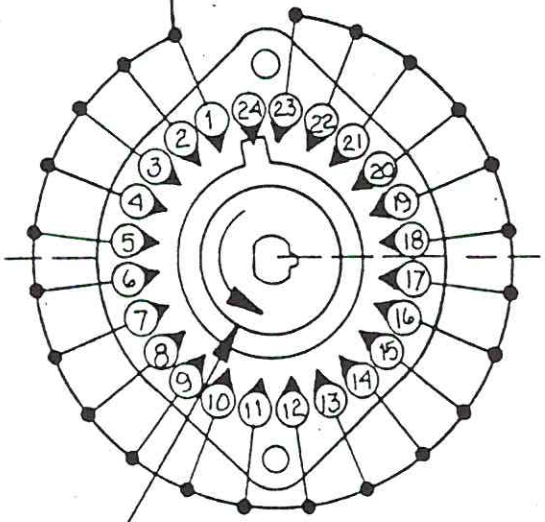
HOME CONTROL WAFER



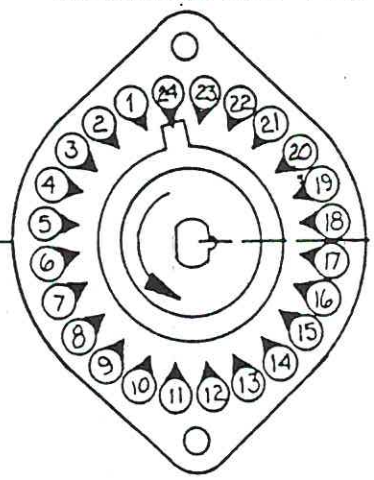
SOLENOID END VIEW



SHAFT END VIEW



CONTROL WAFER SWITCH (24 PORTS)



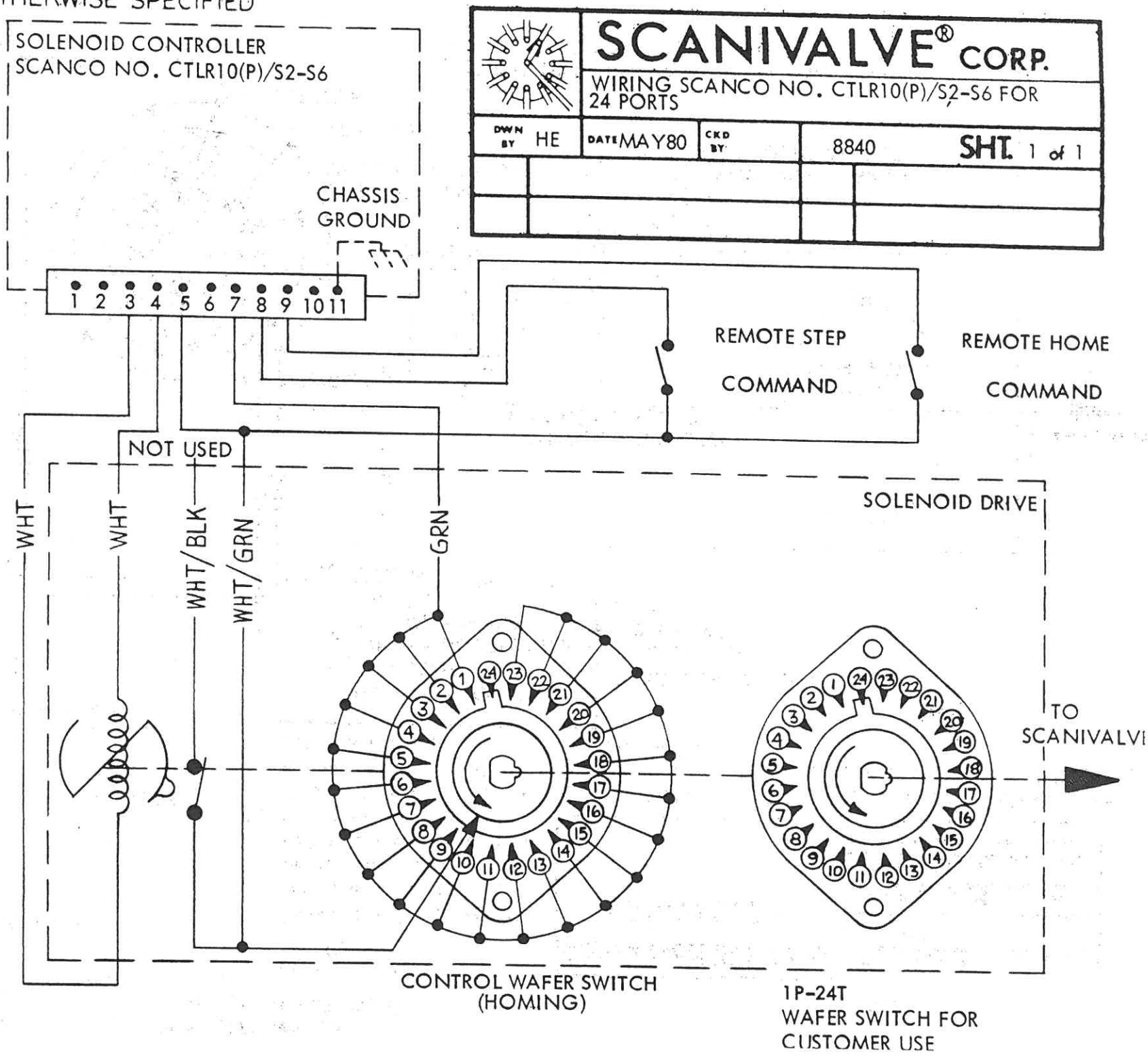
SOLENOID DRIVE

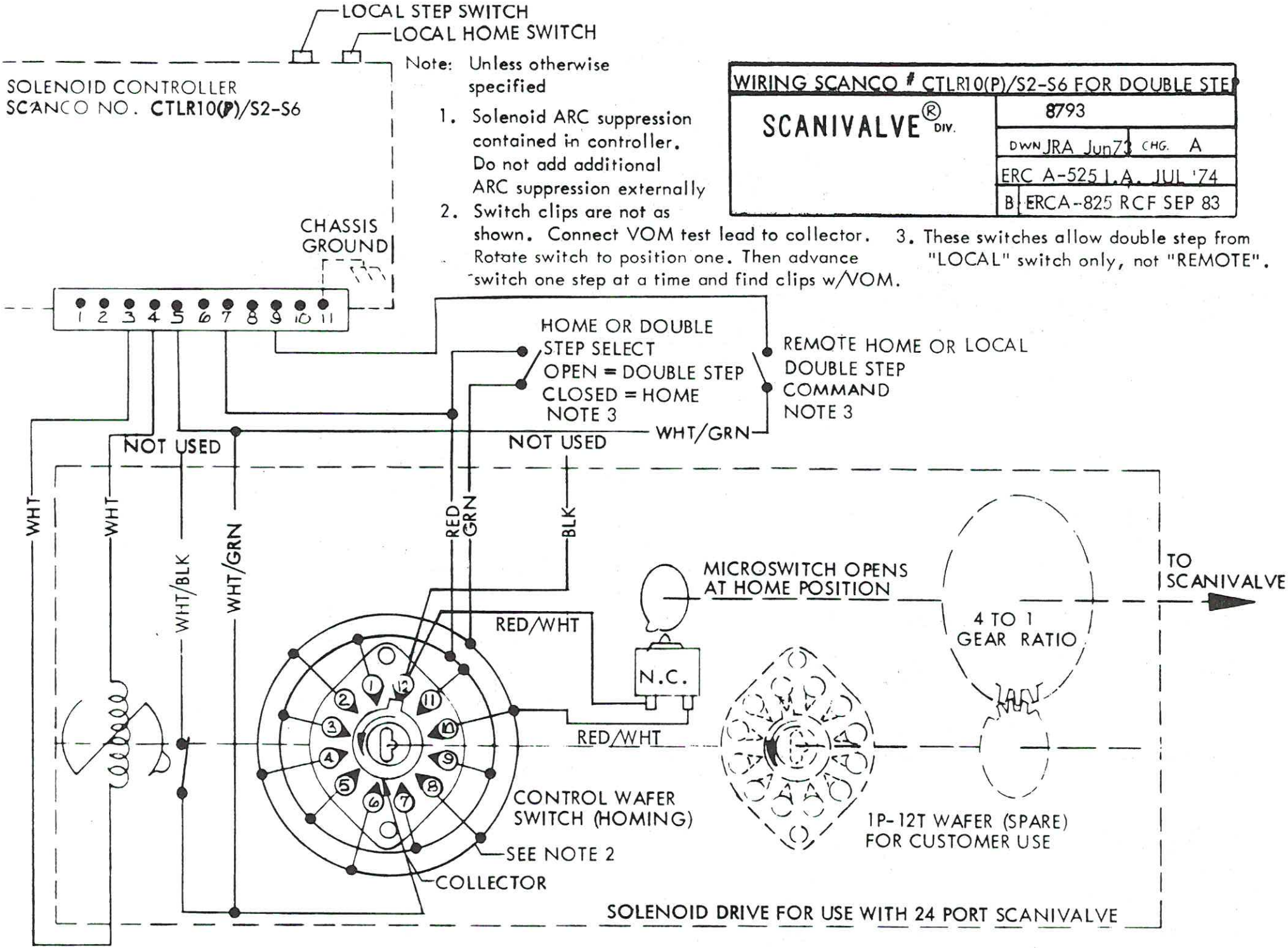
1P-24T WAFER SWITCH FOR CUSTOME USE

TO SCANIVALVE

NOTES: UNLESS OTHERWISE SPECIFIED

1. Solenoid ARC suppression contained in controller. Do not add additional ARC suppression externally.





Note: Unless otherwise specified

1. Solenoid ARC suppression contained in controller. Do not add additional ARC suppression externally
2. Switch clips are not as shown. Connect VOM test lead to collector. Rotate switch to position one. Then advance switch one step at a time and find clips w/VOM.
3. These switches allow double step from "LOCAL" switch only, not "REMOTE".

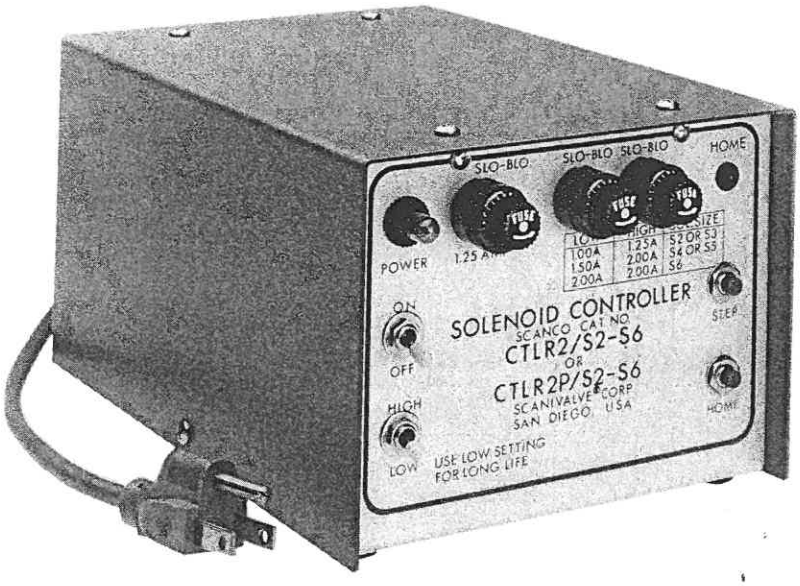
WIRING SCANCO # CTLR10(P)/S2-S6 FOR DOUBLE STEP	
SCANIVALVE® DIV.	8793
	DWN JRA Jun73 CHG. A
	ERC A-525 I.A. JUL '74
	B ERCA-825 RCF SEP 83

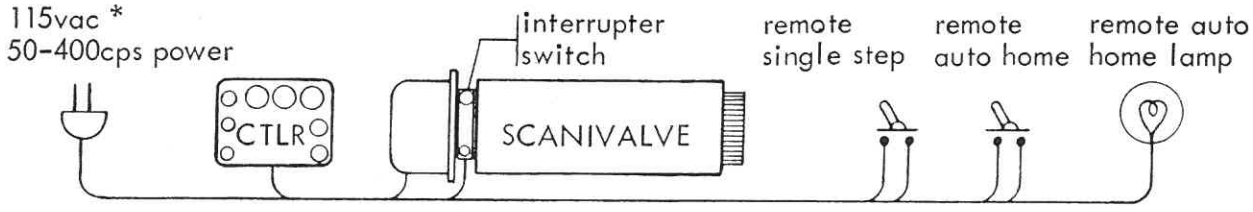
INDEX TO APPENDIX

(SPECIFICATIONS, SPARE PARTS AND ACCESSORIES)

SCANIVALVE CORP.
Post Office Box 20005
San Diego, California 92120
Telephone: (714) 283-0010
Telex: 695023

MODEL CTLR2 SOLENOID CONTROLLER





This solenoid controller was developed to increase the stepping speed of our Ledex solenoid driven Scanivalves.® This is achieved by using pulse length feed back and increased driving voltage. As a by product of this design, the solenoid heating has been greatly reduced per actual solenoid work done.

This solid state controller will drive a size S2 solenoid at 35 steps per second. It will drive a size S6 solenoid at 15 steps per second. Contact the factory on practical step rates for the various solenoid sizes and Scanivalve® loads.

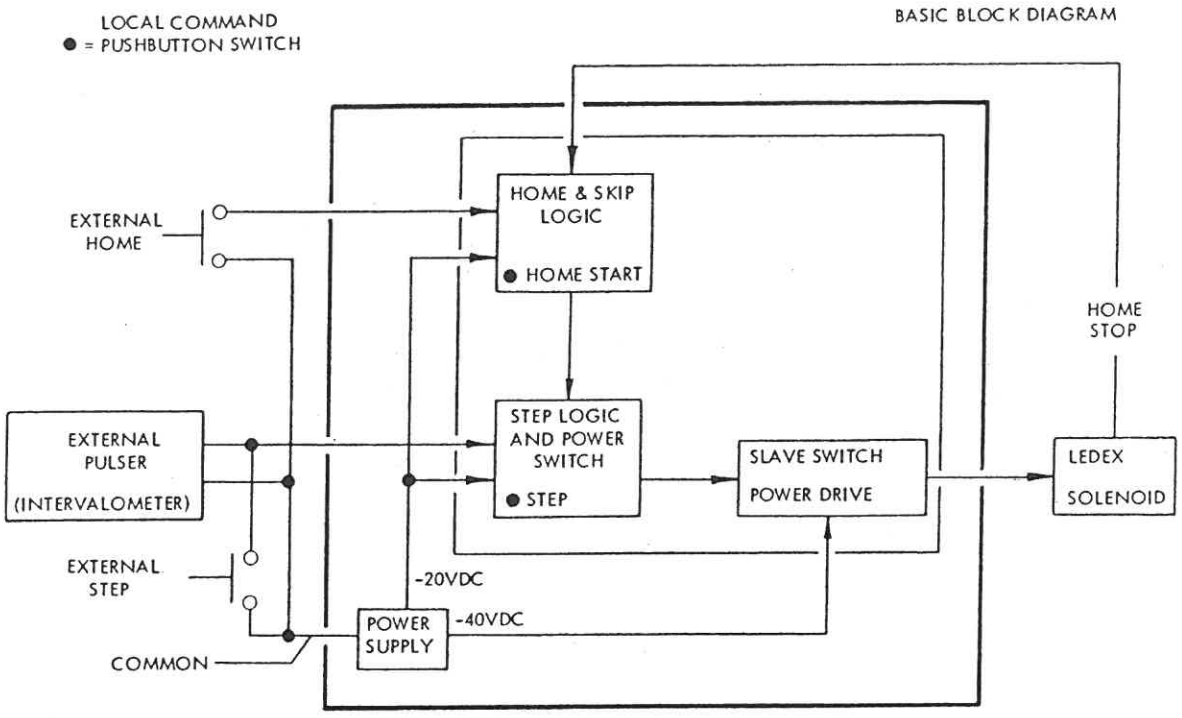
A built-in pulser (intervalometer) is offered for stepping speeds from 30 steps/second to 1 step/2 seconds and 1 step/10 seconds to 1 step/45 minutes, switch selectable range and potentiometer adjustable at rear panel.

The operation of this controller is as follows:
1) The command to advance the Scanivalve® one step is made by an external switch closure of 5 millisecond minimum. A reed switch is well suited to this use. The command circuit is designed so that contact bounce of this switch will not destroy or double this command. At the time of switch closure a bi-stable solenoid driver gates 30 vdc directly to the solenoid terminals. This gate is held open until the cam operated interrupter switch on the Ledex control wafer opens. Two milliseconds after this switch opens, the 30 vdc gate is reset and the controller is now ready to receive a second command. Contact bounce or vibration bounce on the cam operated switch will not cause the 30 vdc gate to reset accidentally.
2) A latching auto-home circuit is provided which requires a 5 ms. minimum switch closure. When used with a 48 position Scanivalve® drive, home position is sensed by means of the standard Ledex solenoid drive switch combination. When given the home command the Scanivalve® is driven at self interrupting speed to the home position. It operates with 24 position drives also.
3) Push buttons for step and home are provided on the box so it can be operated locally. SIZE: 5.40" x 4.15" x 8.50" *220vac also available, please specify on your order.

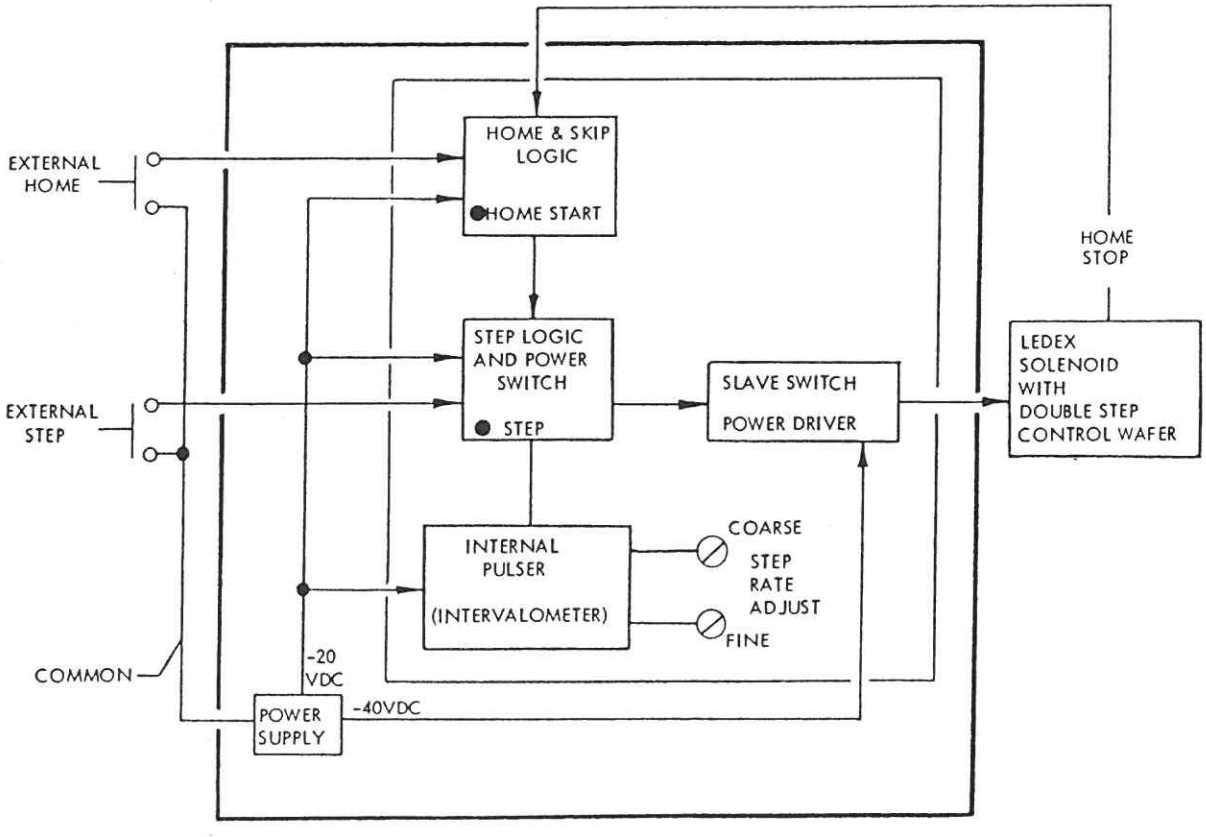
TO ORDER, PLEASE SPECIFY SCANCO NUMBER:

CTLR2/S2-S6 - without pulser
CTLR2P/S2-S6 - with pulser

(over)



CTLR2

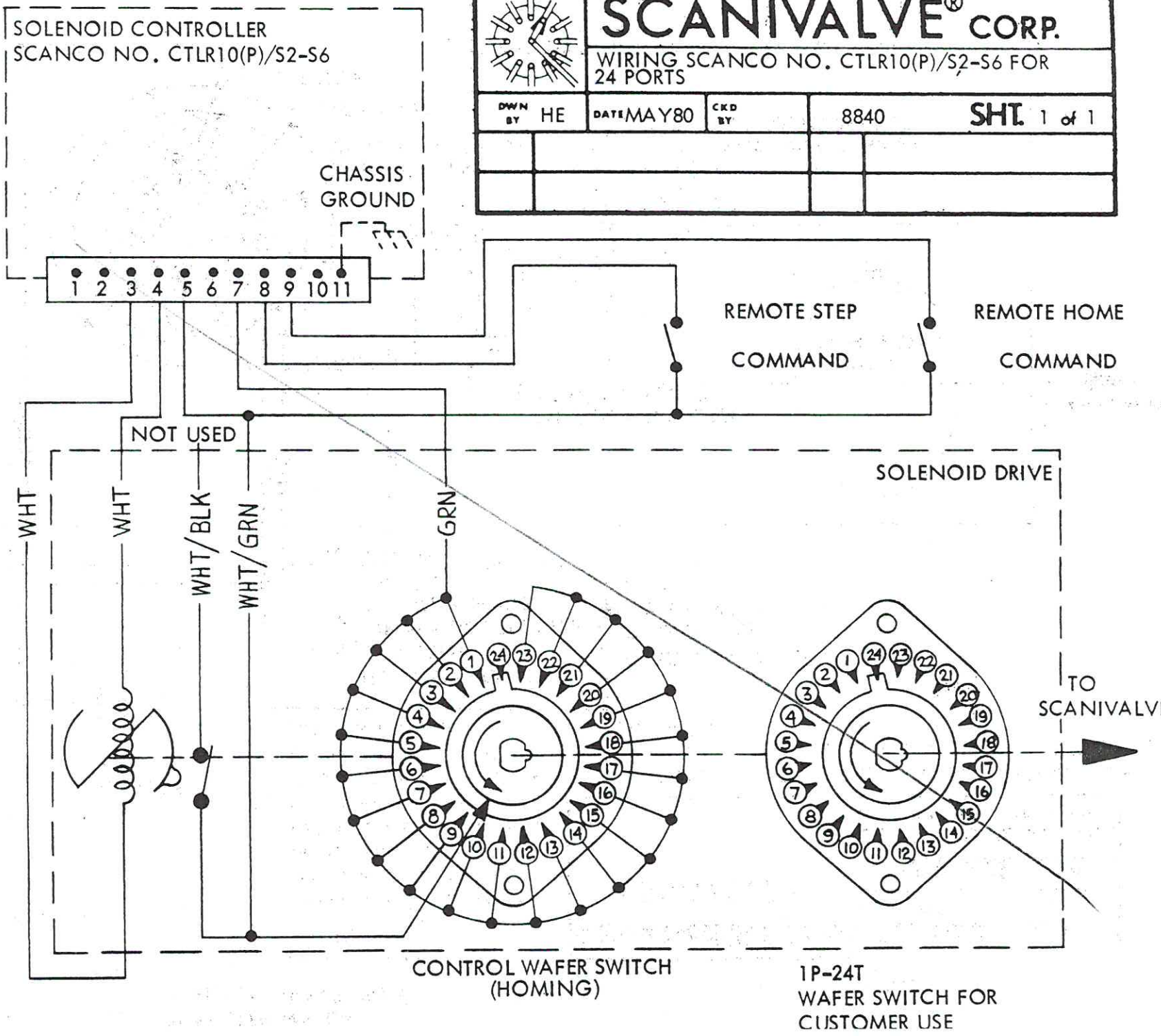


CTLR2P

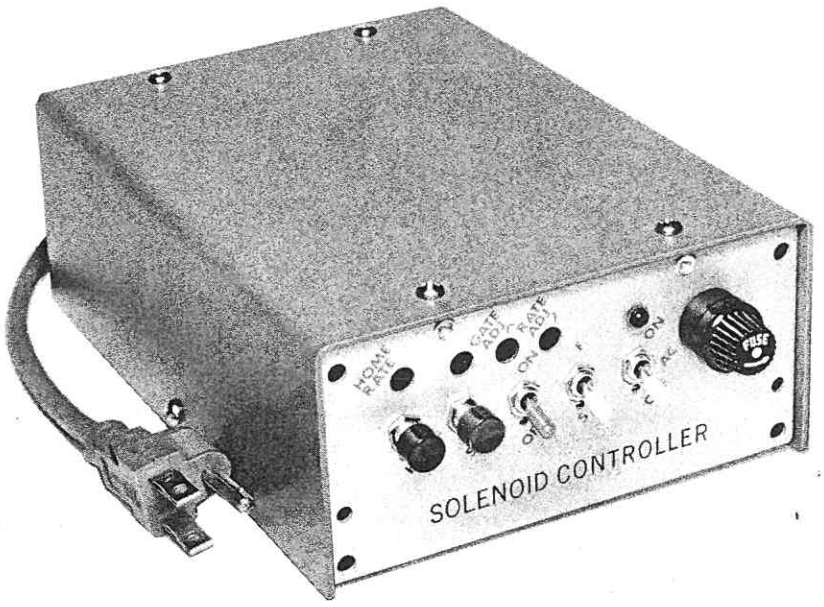
NOTES: UNLESS OTHERWISE SPECIFIED

1. Solenoid ARC suppression contained in controller. Do not add additional ARC suppression externally.

SCANIVALVE® CORP.			
WIRING SCANCO NO. CTLR10(P)/S2-S6 FOR 24 PORTS			
DWN BY HE	DATE MAY80	CKD BY	8840 SHT. 1 of 1



SOLENOID CONTROLLER - WITH PULSER (INTERVALOMETER)



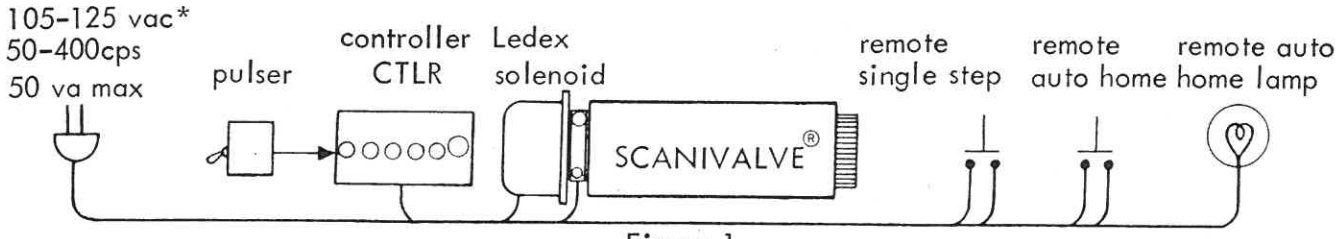


Figure 1

This solenoid controller was developed for applications where the maximum stepping speed of Ledex solenoid driven Scanivalves® is not required. (See model CTLR2). In addition, a built-in pulser (intervalometer) is supplied for stepping speeds from 10/second to 1/30 minutes in two ranges, switch selectable and potetiometer adjustable.

The controller operates open loop and does not require the solenoid to be equipped with an auto-interrupter switch. This design has the advantage of eliminating the arcing (explosion hazard) which normally accompanies the use of auto interrupters with other controllers.

The step rate is dependent on size of solenoid and the load driven. The CTLR10P is not recommended for use with S5 and S6 solenoid drives when using W62 wafers at scan rates greater than 2 ports/sec. It may be used when wired per Figure 10.01 in CTLR10P Instruction Manual providing the scan rate is less than or equal to 2 ports/sec. Scanivalve® using a CTLR2 (or-2P) for maximum S5 and S6 drive performance.

- Continuous duty	= 2 to 6 steps/second
- Homing rate	= 2 to 20 steps/second. Adjustable by user.
Time required to advance one step	= 10 to 100 ms. Adjustable by user.
Step & Home input commands	= 5 ms minimum, switch or NPN transistor closure to signal common.
Package dimensions	= 5.1" wide x 2.7" high x 8.3" long

* For 210-250 vac - specify on order:

TO ORDER, PLEASE SPECIFY SCANCO NUMBER: CTLR10P/S2-S6

(over)

● = LOCAL COMMAND
● = PUSHBUTTON SWITCH

BASIC BLOCK DIAGRAM

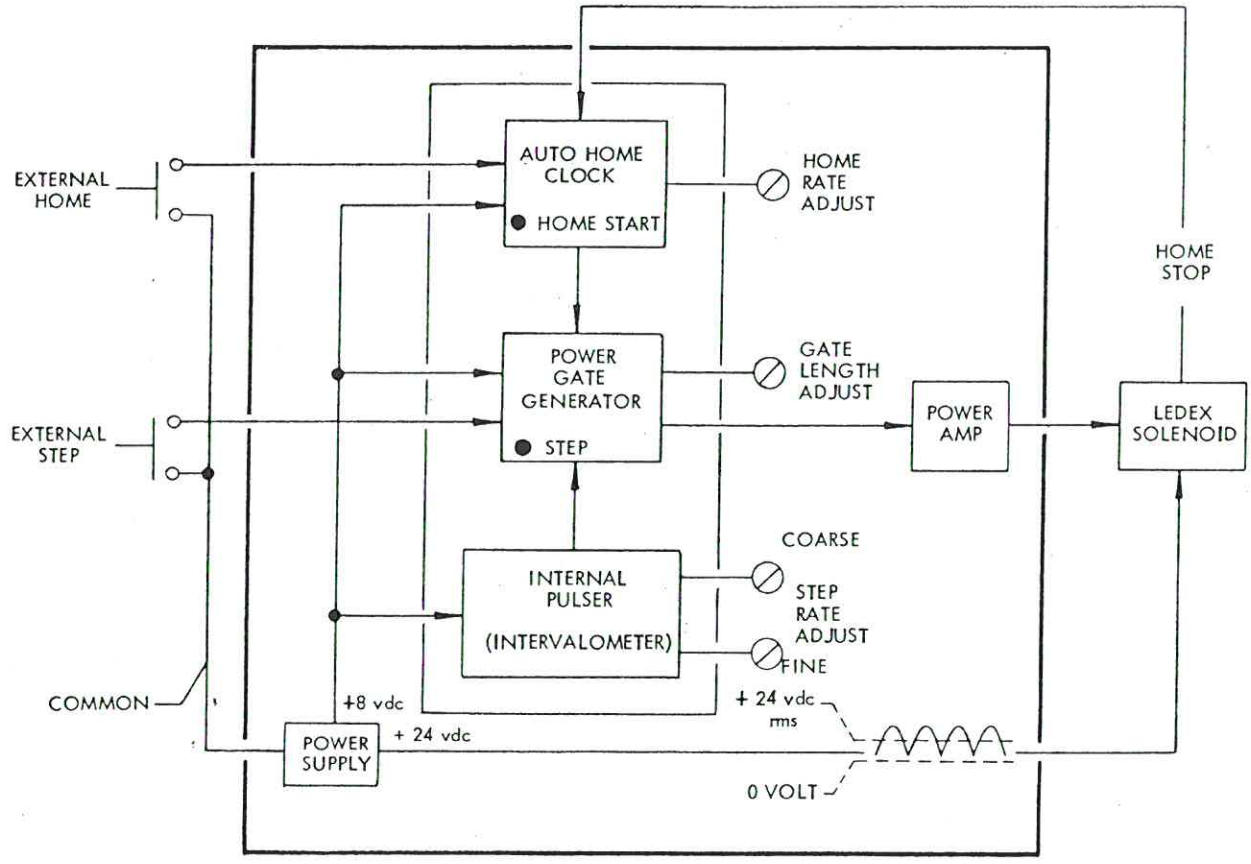


FIGURE 2(CTLR10P)

INDEX TO APPENDIX

(THEORY)

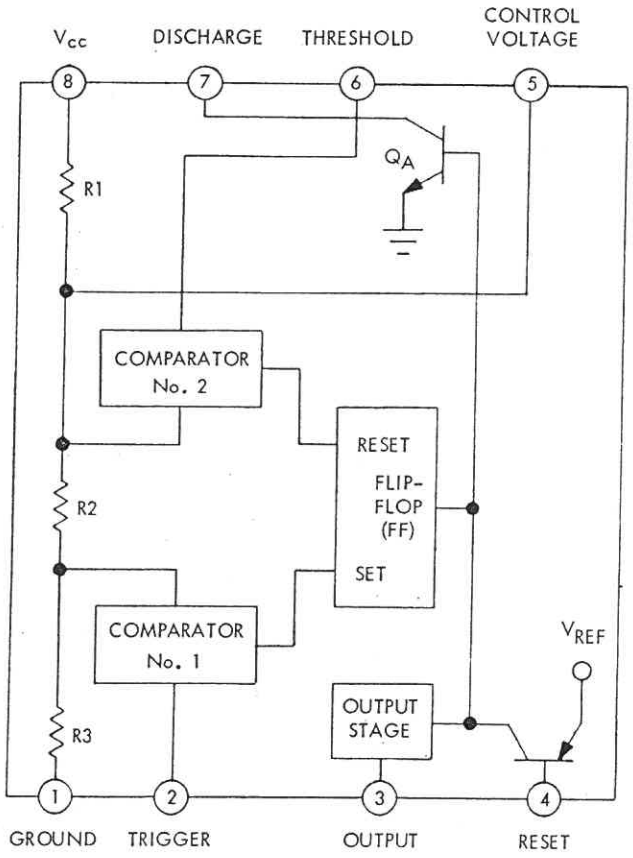
SCANIVALVE CORP.
Post Office Box 20005
San Diego, California 92120
Telephone: (714) 283-0010
Telex: 695023

ASTABLE AND MONOSTABLE MULTIVIBRATORS

USING AN IC (MONOLITHIC) TIMING CIRCUIT

The use of a single IC (monolithic) timing circuit to perform Astable and Monostable functions reduces the number of components necessary to implement the functions and increases the reliability of the finished product. We have found it possible to build circuits with periods in excess of one hour using one megohm timing resistors and 500 to 1000 ufd timing capacitors. The primary trade-off is between current thru the timing resistor versus leakage current of capacitors in this capacitance range. Too low a resistor current (e.g. current thru a 20 megohm resistor) and/or too high a capacitor leakage current (e.g. 5 or 10 ua in a capacitor of this size) prevents the capacitor from charging to the threshold voltage of the timing circuit.

Figure 1 shows the block diagram of a typical monolithic timing circuit. The circuit elements shown are fabricated on the same monolithic semiconductor chip. The chip is packaged in standard 8-lead IC (integrated circuit) packages (e.g. TO-5, dual-inline, etc.).



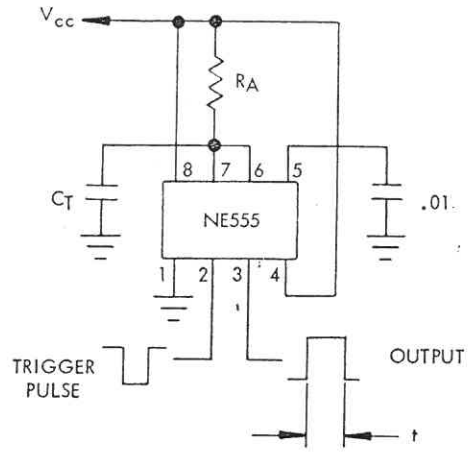
BLOCK DIAGRAM, IC (MONOLITHIC) TIMING CIRCUIT

FIGURE 1

R1 = R2 = R3 $\approx$ 5K nominal. These resistors form a voltage divider that supplies the reference voltages to the comparators. The process used in manufacturing the chip may allow absolute resistance tolerances of 10 to 30%, but the ratios of resistors to each other and to the total resistance can be held to 2% or less. The reference voltages are therefore a relatively fixed percent of V_{cc} and account for the exceptional temperature and ΔV_{cc} stability coefficients of the circuit. Typical timing errors due to the IC are:

1. 50 ppm/°C.
2. 100 ppm/V (ΔV_{cc}). When the timing capacitor is charged thru a resistor(s) to V_{cc}.

Figure 2 shows a typical monostable multivibrator using the IC.



$t = -RC\ (\ln 1/3) = 1.1\ R_A C_T$

BASIC MONOSTABLE MULTIVIBRATOR

FIGURE 2

In the circuit's quiescent state: Refer to Figure 1 & 2.

1. The trigger input (pin 2) is high.
2. The FF is in its reset state.
3. The reset input (covered separately) is tied to V_{cc} to avoid any possibility of false triggering.
4. The output is low.
5. The timing capacitor (C_T) is discharged and Q_A is on.
6. The capacitor at the control voltage input (pin 5) prevents erratic timing errors due to noise.

The sequence of operation is:

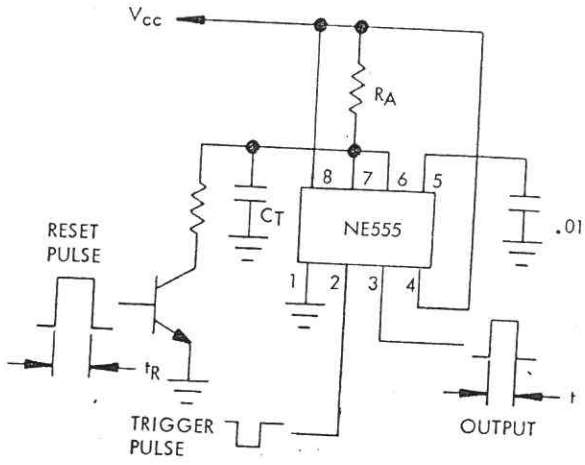
1. A negative going pulse is applied at the trigger input (pin 4). When this input decreases below the reference voltage for comparator No. 1, the FF is set.
2. When the FF is set, the output goes high, Q_A turns off and the timing capacitor (C_T) charges towards V_{cc} thru R_A.
3. When the voltage across C_T (sensed by comparator No. 2 via pin 6) exceeds the reference for comparator No. 2, the FF is reset.
4. This causes the output to go low and the timing capacitor to be discharged by Q_A.
5. The length of the output pulse is given by

$$t = -RC(\ln 1/3) = 1.1\ R_A C_T.$$

In our applications the reset input has primarily been used for disabling astable multivibrators. When the reset input is low, Q_A conducts (discharging C_T) and the output goes low. This characteristic limits the variety of applications since in most monostable and

pulse stretching circuits it is undesirable for the output to go low until the entire timing cycle is completed.

Figure 3 shows a pulse stretcher which has a transistor added for the reset control thus avoiding this characteristic.



$t = 1.1\ R_A C_T$ + SUM of t_R's

BASIC MONOSTABLE WITH RESET (BASIC PULSE STRETCHER)

FIGURE 3

The difference in operation between the circuits of Figures 2 and 3 is that the output pulse is "stretched" by the reset pulse. The length of the output pulse is given by

$$t = 1.1\ R_A C_T + t_{RESET}$$

where t_{RESET} = the sum of the reset pulse duration(s).

Figure 4 shows an Astable Multivibrator using the reset input for the enable input.

In the circuit's quiescent state (circuit disabled): Refer to Figures 1 and 4.

1. The reset input is grounded thru S1.
2. Q_A is on, the output is low and the voltage across C_T is $\approx$ zero.
3. The capacitor at the control voltage input (pin 5) prevents erratic timing errors due to noise.
4. The trigger input is low since it is tied to pin 7 (Q_A collector) thru R_B.
5. The FF is set.

The sequence of operation is:

1. S1 is switched to enabled, allowing C_T to charge to V_{cc} thru R_A and R_B. Since C_T is in a discharged state at the beginning of this cycle, the first output pulse will be longer than the rest of the pulses by the time it takes for C_T to charge to 33% V_{cc}.
2. The output goes high at the same time that C_T starts charging.
3. When the voltage across C_T exceeds the threshold voltage, comparator No. 2 resets the FF and the output goes low causing C_T to discharge thru R_B to ground.
4. The duration of the high output pulse is:

   A. On the first pulse:

   $$t_1 = -RC(\ln 1/3) = 1.1\ (R_A + R_B)\ C_T.$$

   B. On the second and subsequent pulses:

   $$t_1 = -RC(\ln 1/3 - \ln 2/3) = -RC(\ln 0.5) = 0.693(R_A+R_B)C_T$$

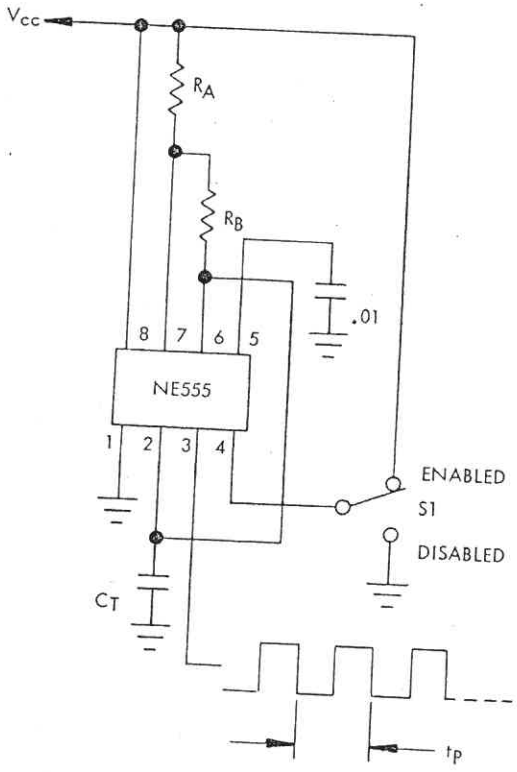
5. The output stays low until C_T discharges to less than the trigger level. When C_T discharges below the trigger level, the FF is set and C_T charges towards V_{cc}.
6. Since C_T discharges only thru R_B, the duration of the low output pulse is:

   $$t_2 = -RC(\ln 0.5) = 0.693\ R_B C_T.$$

7. The total period after the first cycle is given by:

   $$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)C_T.$$

8. The cycles repeat until the multivibrator is disabled by switching S1 to ground. When this is done the output goes to zero, C_T discharges to ground and the FF is set.
9. Note that only when $R_B >> R_A$ is the output nearly symmetrical. Symmetry can be established for all practical purposes (difference $\leq$ 1%) by making $R_B \geq 100\ R_A$.



$t_P = -RC(\ln 0.5) = 0.693(R_A+2R_B)\ C_T$

BASIC ASTABLE MULTIVIBRATOR

FIGURE 4

SET-RESET FLIP-FLOP

(SR FF)

The SR FF is a device having two stable states and two types of input signals (i.e., SET and RESET inputs) each of which corresponds with one of the two states. It has two complementary outputs (i.e., when one output is low the other output is high). The output which is TRUE or "1" immediately following a SET input is labeled Q and the other output, which is FALSE or "0" is labeled $\overline{Q}$ (read Q bar or not Q). Positive feedback is used to provide the latching and fast transition from one state to the other which is characteristic of this type of FF.

An SR FF has one or more SET and RESET inputs and one or more Q and $\overline{Q}$ outputs. If only one output is used, it is still necessary to have both types of inputs.

One of the FF reset terminals is normally used for an INITIAL CLEAR function. This function insures that all of the FF's in a circuit are in an initial (or desired state) following application of power to the circuit.

Figure 1 shows an example of a basic discrete component SR FF with switches to represent possible inputs to the FF.

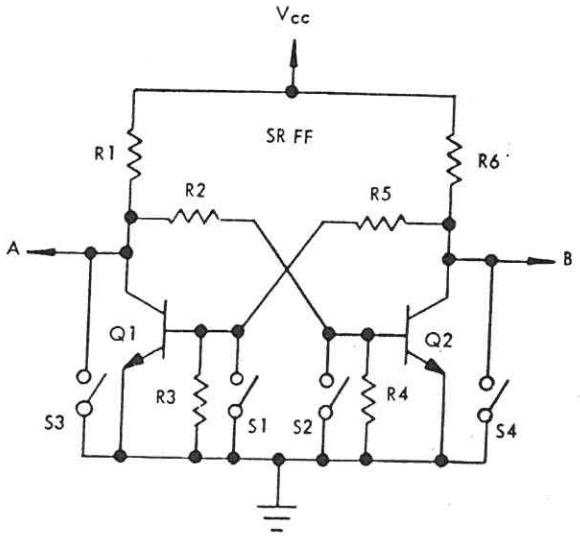


FIGURE 1

S1 and S2 are low level base inputs. This type of input is relatively noise sensitive and not normally used in industrial applications. S3 and S4 represent collector inputs. This type of input is less noise sensitive than the base type since it requires the switching of larger voltages and currents, and is not as sensitive to off-set voltages due to diodes etc. (in the input circuit). If S1 or S4 is designated the SET input, then output A is called the Q output.

Assume quiescent conditions are such that: Q1 is on and Q2 is off; S4 is the SET input & S3 is the RESET input; A is the Q output & B is the $\overline{Q}$ output. When S4 is closed the signal is coupled through R5 to the base of Q1. Q1 turns off and its collector goes high. This is coupled through R2 to the base of Q2 and Q2 turns on causing its collector to go low. When S4 is opened the collector of Q2 will stay low which in turn will cause Q1 to stay off. The circuit will now stay in this state until a reset signal is applied at the collector of Q1 (i.e., S3 is closed). When S3 is closed, the reverse action occurs and the circuit will stay in the reset state until another SET input occurs.

The discrete component SR FF is normally used in very high noise environments and/or when only a couple of FF's are needed in a circuit. When several FF's are needed and when their noise immunity is acceptable cross-coupled NAND or NOR gates are normally used.

Figure 2 shows an RS FF implemented with 3-input NAND gates and its equivalent logic symbol.

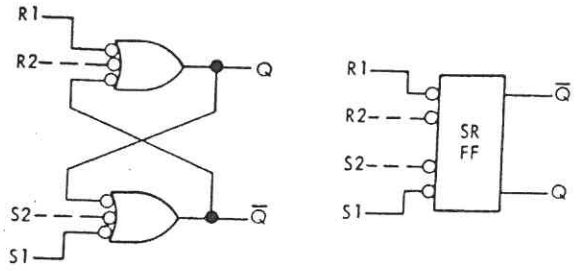


FIGURE 2

Since 2, 3, 4, & 8 input NAND and NOR gates are easily available it can be seen that, assuming one R and S input is reserved for cross coupling, there can be from one to seven R and/or S inputs. Although the type of gates used must be the same (both NAND's or both NOR's) the number of inputs to each gate does not have to be equal (e.g., a 2-input NAND and an 8-input NAND can be cross-coupled to form an RS FF with one SET input and seven RESET inputs or vis-a-vis).

Figure 3 shows an SR FF implemented with 3-input NOR gates and its equivalent logic symbol.

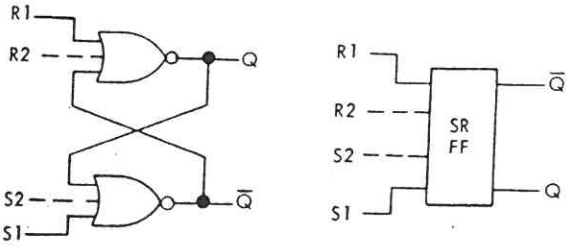


FIGURE 3

It should be noted that NAND gates require inputs to go low for operation while NOR gates require inputs to go high. The Q output is still the high output following a SET input.

Although it is possible to obtain integrated circuit packages, with up to four or more RS FF per package, it is still often desirable to use the above circuits because of packaging or economic reasons. When multiple RS FF I.C.'s are used, the number of available inputs is usually limited to one SET and one RESET and only the Q output is usually available for each of the FF's in the I.C.

The outputs have been defined as Q = 1 following a SET input and Q = 0 following a RESET input. The output is considered undefined for both a SET and a RESET input applied at the same time.

APPENDIX B

ASSIGNMENT OF LOGIC LEVELS TO BINARY LOGIC ELEMENTS

20.1 A single arrangement of hardware may perform both the AND function or the OR function. This functional duality is employed in numerous single device, as well as multi-device systems.

The following tables and their related paragraphs develop the convention of considering the AND function as an element whose output is "active" when all its inputs are "active". Any AND input "nonactive" will produce a "nonactive" output. The OR function is considered an element whose output is "active" when any one or more input(s) are "active". All OR inputs "nonactive" will produce a "nonactive output".

Note that the above activity definitions do not refer to logical one, logical zero or electrical reference states.

To identify the activity of a device selected to implement the logic, the state condition of active input(s) and the resultant active output are identified by the presence or absence of active state signal indicators (small circles) at the input(s) or output of logic functions (AND/OR).

These graphic representations as well as English notations are employed to illustrate the relationship of specific functions operating individually or interconnected to perform machine functional operations as a system.

A small circle at the input(s) indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

A small circle at the symbol output side indicates that the output of the activated function is relatively low (L). Absence of a small circle at the symbol output indicates that the output of the activated function is relatively high (H).

The presence of an indicated active output does not necessarily provide a useful input to other elements. It may prevent the operation of some and enable others. Conversely, the absence of the indicated output signal state may provide a useful input to elements in the logical net and prevent the operation of others.

Activating input(s) or an activated output of a function may be (a) logical "one" in either the more positive high state (H) or the less positive low state (L), (b) a logical "zero" either high or low, or (c) a mixture of both "one" or "zero" either high or low.

20.2a Consider a device whose active output (F) is a function of two signals (A, B). The output and both input levels are capable of assuming only the arbitrarily chosen values, +2 volts (High "H") and -3 volts (Low "L"). The circuit behaves according to Device Activity States Table 1 below.

Substitution of mnemonic abbreviation "H" for the +2V levels and "L" for the -3V levels in Table 1 results in Activity Combinations Table 3 below.

When the +2V level is considered the activating level and is assigned the logic value 1 and the -3V level is considered the inactive level and is the logic value 0, substitution of these logic state values for the Table 1 active voltage levels results in AND Function Activity States (Internal) Table 2. The device is now said to perform the AND function and is symbolized without level indicators.

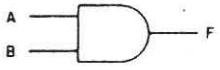


Fig. 1

20.2b Consider the same device behaving according to Table 1.

Substitution of mnemonic abbreviation "H" for the +2V levels and "L" for the -3V levels in Device Activity States Table 1 results in Activity Combinations Table 3 below.

When the -3V level is considered the activating level and is assigned the logic value 1 and the +2V level is considered the inactive level and is the logic value 0, substitution of these logic state values for the Table 1 active voltage levels results in OR Function Activity States (Internal) Table 4. The device is now said to perform the OR function and is symbolized with active level indicators.

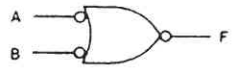


Fig. 2

Note upon comparison of Tables 2 and 3 with Tables 4 and 3, that logical "one", the active level, has been High for AND and Low for OR. Logic value one has been assigned to active presence signals.

AND Function Activity States
Table 2

Input		Output
A	B	F
1	1	1
1	0	0
0	1	0
0	0	0

(Electrical Truth)
Device Activity States
Table 1

Input		Output
A	B	F
+2V	+2V	+2V
+2V	-3V	-3V
-3V	+2V	-3V
-3V	-3V	-3V

Activity Combinations
Table 3

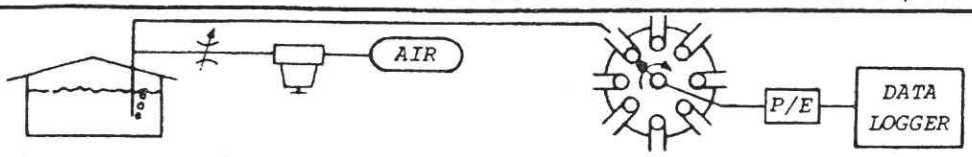
Input		Output
A	B	F
H	H	H
H	L	L
L	H	L
L	L	L

OR Function Activity States
Table 4

Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

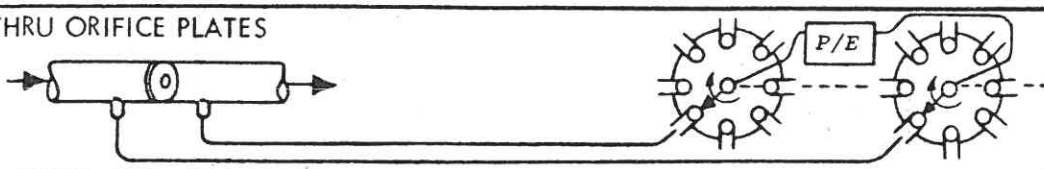
SOME TYPICAL SCANIVALVE® APPLICATIONS ASK FOR SA/ST NO. ___

TANK LEVEL



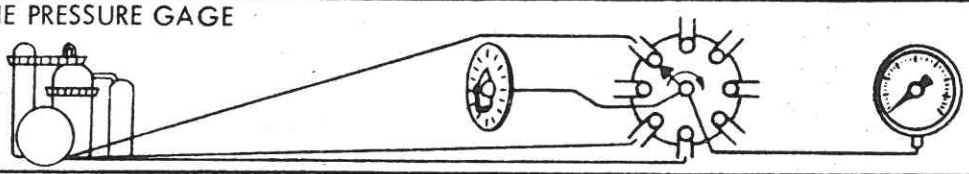
SA NO.2

FLOW THRU ORIFICE PLATES



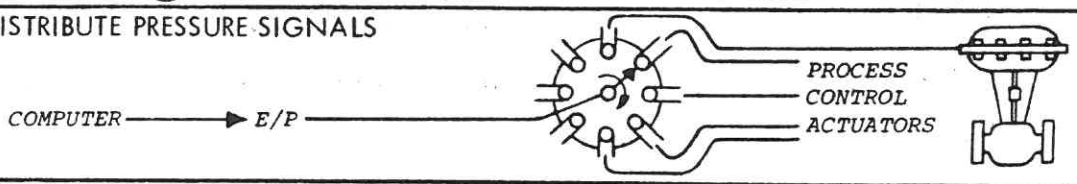
SA NO.3

SHARE ONE PRESSURE GAGE



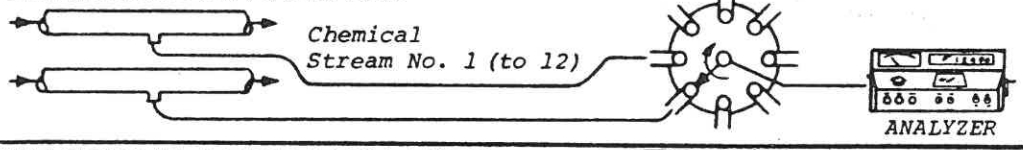
SA NO.5

DISTRIBUTE PRESSURE SIGNALS



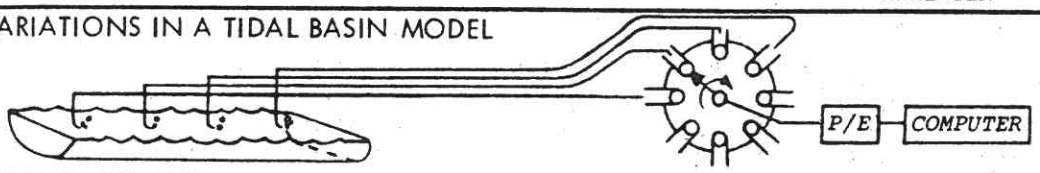
SA NO.6

SAMPLE MULTIPLEXER FOR ANALYZERS



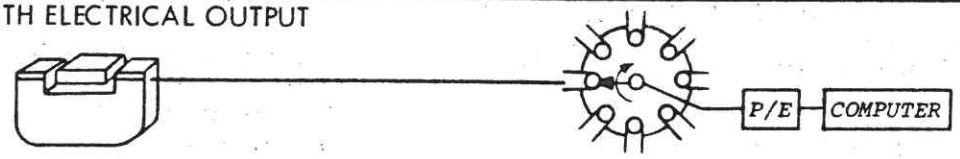
SA NO. 8

TIDAL VARIATIONS IN A TIDAL BASIN MODEL



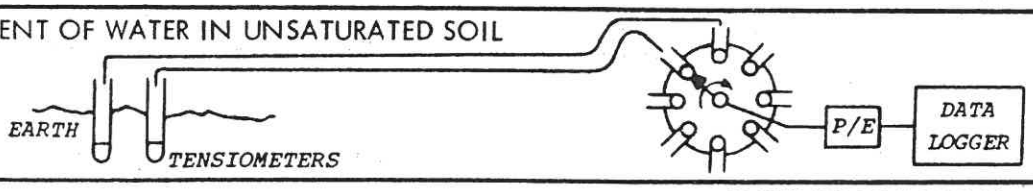
SA NO.9

AIR GAGES WITH ELECTRICAL OUTPUT



SA NO.10

MOVEMENT OF WATER IN UNSATURATED SOIL

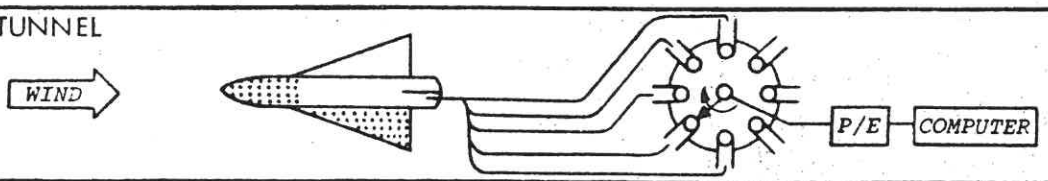


SA NO.11

REMOTE$_{electrical}$ CONTROL ROOM$_{pneumatic}$ OPERATION BY < PRESSURE SCANNING / PRESSURE DISTRIBUTING

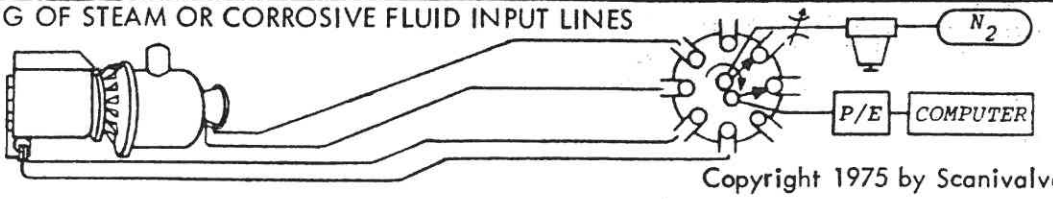
SA NO.12

WIND TUNNEL



SA NO.13

PURGING OF STEAM OR CORROSIVE FLUID INPUT LINES

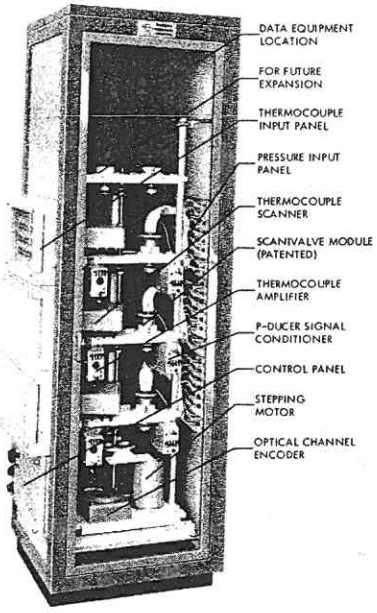


ST NO.7

SCANIVALVE CORP. P.O. BOX 20005, SAN DIEGO, CALIFORNIA 92120
TEL: (619) 283-0010 OR 283-5851 TELEX: 695023

0-500 PSI APPLICATIONS

MSS-48C



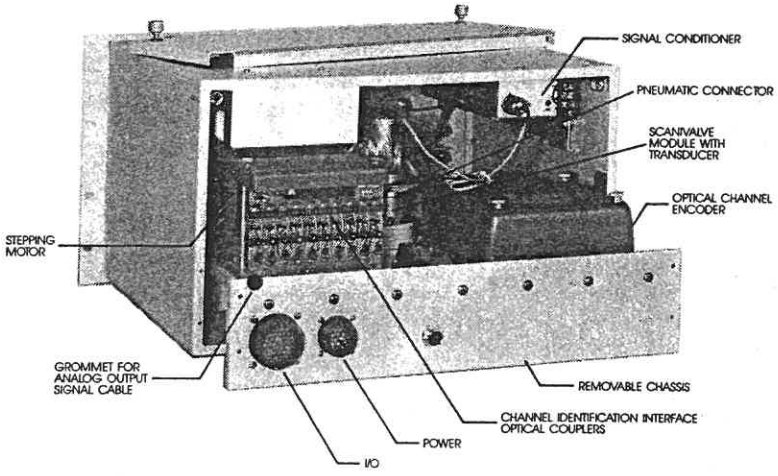
MULTIPLE SCANIVALVE® SYSTEM

The photo at left shows our Multiple Scanivalve System. The left side of this cabinet shows three electrical (thermocouple) scanner panels with three air sequencers for scanning 144 temperatures. The right side shows three pressure input panels with three pressure scanners for 144 test pressures. The cabinet still has two blank input spaces, into which either pressure or temperature panels with scanners or sequencers can be installed in the field. The common stepper drive can drive up to 12 Scanivalve modules to scan 576 pressures, or 12 air sequencers to scan 576 temperatures.

The first 48 MSS was shipped to Rolls Royce in 1964. This computer input scanner (multiplexer) has been transducing over 500 jet engine test pressures since installation.

For more information, send for our MSS-48C brochure.

SSS-48C



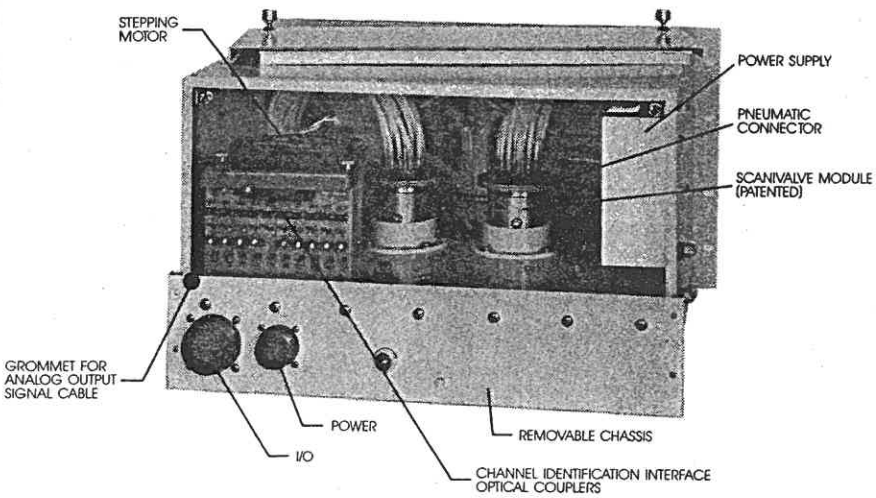
SINGLE SCANIVALVE SYSTEM

The photo at left shows our Single Scanivalve System. It contains a stepper drive, optical channel encoder, and one Scanivalve module. The pressure input panel is identical with the input panels discussed above. This single system can be located near the pressures and controlled by the computer thousands of feet away; or it can be teamed up with a mini-computer at a local test area.

The first 500 psi Scanivalve was sold to Aerojet General Corp. for rocket nozzel research in 1958. Since that time, hundreds of these SSS units have been used for computer interfacing or "data research."

For more information, send for our SSS-48C brochure.

DSS-24/48C



DOUBLE SCANIVALVE SYSTEM

The photo at left shows our Double Scanivalve System. It is identical to the SSS except for the relocation of the channel encoder and the second Scanivalve. The DSS is used for scanning differential pressure pairs across pitot tubes, orifice plates, etc.

For more information, send for our DSS-24C brochure.